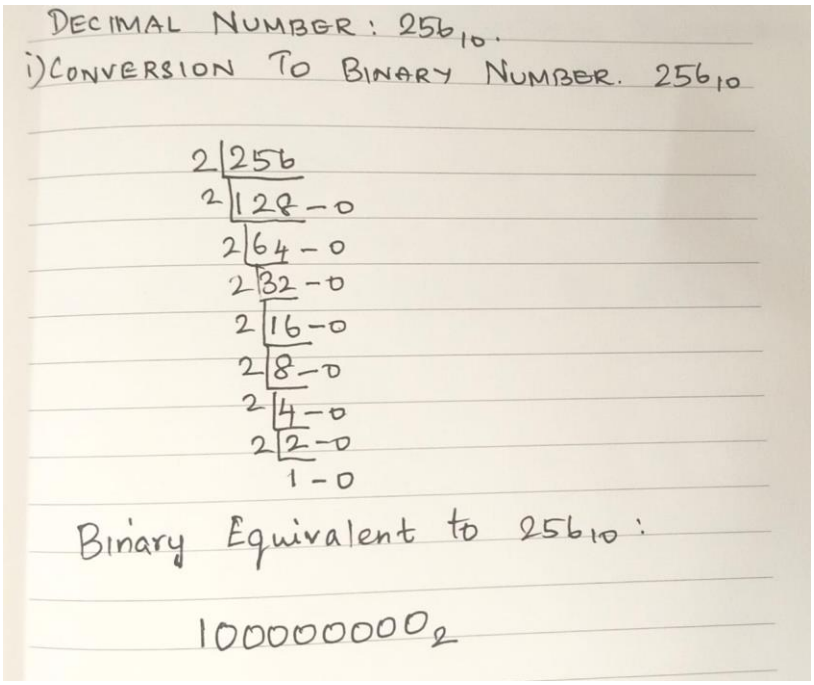
1324

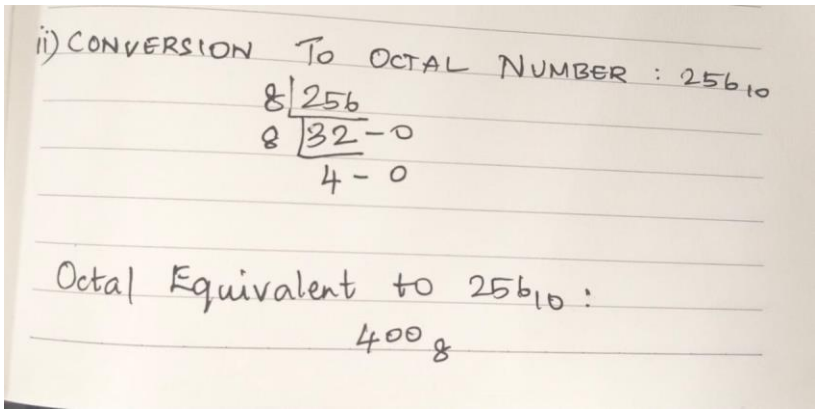
DIGITAL LOGIC DESIGN

1 (a) Convert the decimal number (256)10 into its equivalent binary number, octal number, and hexa-decimal number.

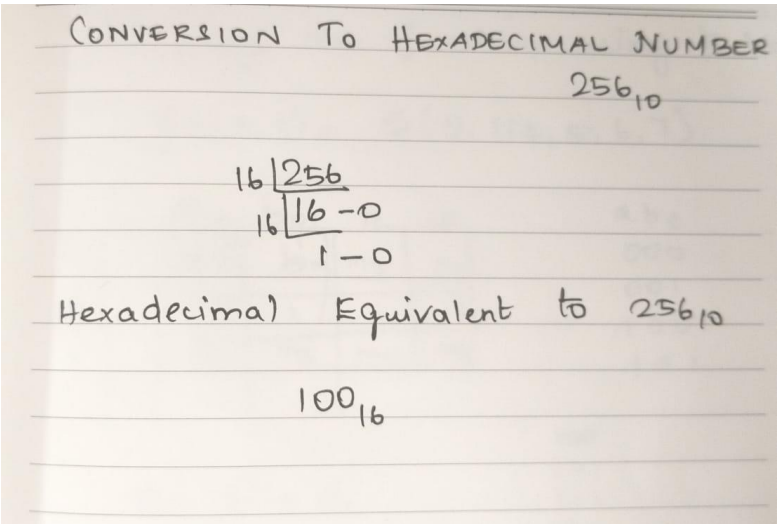
BINARY CONVERSION



OCTAL CONVERSION



HEXADECIMAL CONVERSION



1 (b) Discuss Any two Binary Code Standards. **(5 Marks each)**

(i) Binary Coded Decimal:

Binary Coded Decimal**,** or BCD**,** is another process for converting decimal numbers into their binary equivalents.

The BCD equivalent of a decimal number is written by replacing each decimal digit in the integer and fractional parts with its four bit binary equivalent. The BCD code is also known as 8421 BCD code, with 8,4,2 and 1 representing the weights of different bits in the four-bit groups.

Truth Table for BCD:

Binary Number	BCD Equivalent
0	0000
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001

Ex: Convert (324)10 in BCD

(324)10 -> 0011 0010 0100 (BCD)

Again from the truth table above,
3 -> 0011
2 -> 0010
4 -> 0100
thus, BCD becomes -> 0011 0010 0100

Advantages:

- It is a form of binary encoding where each digit in a decimal number is represented in the form of bits.
- This encoding can be done in either 4-bit or 8-bit (usually 4-bit is preferred).
- It is a fast and efficient system that converts the decimal numbers into binary numbers as compared to the existing binary system.

(ii) ASCII:

The American Standard Code for Information Interchange, or ASCII, is a character encoding standard. ASCII is a 7-bit or 8-bit code used to represent characters such as letters, digits, symbols, and control characters (like newline or backspace). It assigns a unique binary code to each character.

- ASCII is a 7-bit or 8-bit code used to represent characters such as letters, digits, symbols, and control characters (like newline or backspace).
- It assigns a unique binary code to each character.
- Extended ASCII uses 8 bits (1 byte), allowing for 256 characters.

Examples:

Character	Keyboard Character	ASCII Value
Space	(space)	32
Exclamation Mark	!	33
Quotation Mark	“	34
…	…	…
Uppercase A	A	65
Uppercase B	B	66
…	…	….
Lowercase A	a	97
Lowercase B	b	98
…	…	….

ASCII characters are represented in binary, providing a machine-readable format that computers use for internal processing.

● 7-bit ASCII supports 128 characters (0 to 127 in decimal).

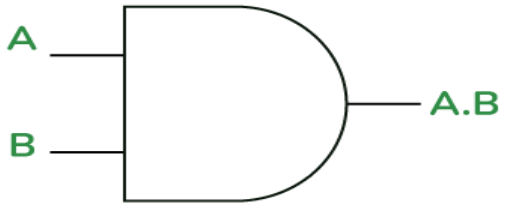
● 8-bit Extended ASCII includes additional symbols and characters (128 to 255).

1 (c) Explain the AND, OR, NOT Gates.

AND Gate:

AND gate is the fundamental logic gate that executes the logical multiplication of binary input. When all the inputs are 1, the AND Gate outputs 1, otherwise it outputs 0. A dot (.) denotes the AND operation.

2- Input AND Gate



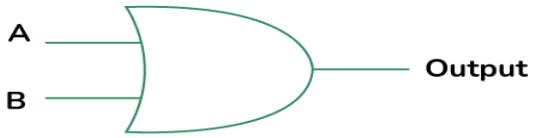
Truth Table

A (Input 1)	B (Input 2)	X = (A.B)
0	0	0
0	1	0
1	0	0
1	1	1

OR Gate:

OR gate is the fundamental logic gate that executes the logical addition of binary input. When any one of the inputs is 1, the OR Gate outputs 1, otherwise it outputs 0. A Plus (+) denotes the OR operation.

2-Input OR Gate



Truth Table

Input A	Input B	Output
0	0	0
0	1	1
1	0	1
1	1	1

There is a basic difference between logical operations of AND & OR Gate AND gate produces high output when both inputs are high means 1, whereas the OR gate produces output as binary 1 when either of the inputs is 1 or it will give 0 as output.

NOT Gate:

Truth Table

A (Input)	Y = Ā (Output)
0	1
1	0

NOT gate is a basic logic gate having only a single input and a single output. The output of the NOT gate is logic 0 when its input is logic 1 and the output is logic 1 when its input is logic 0. Thus, the NOT gate is used to perform the inversion operation in digital circuits. It complements the input and produces a corresponding output. Being a basic logic gate, the NOT gate is used in a variety of digital circuits to design and implement their basic logic circuits.

The Boolean expression of NOT Gate is as follows:

$Y = \bar{A}$

or

$Y = A'$

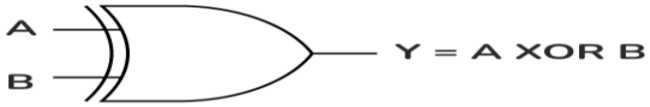
1 (d) Realize Ex-OR and AND gate using NOR Gate.

XOR Gate Realization using NOR Gate: **(5 Marks each)**

XOR gate is a logic gate that results in an output high with an odd number of high inputs. In other words, if the number of 1's is odd in the input then, the output of XOR is 1. XOR gate gives output 1 when all the inputs are different. XOR Gate is denoted by $\oplus$

$A \oplus B = A'B + AB'$

XOR Gate

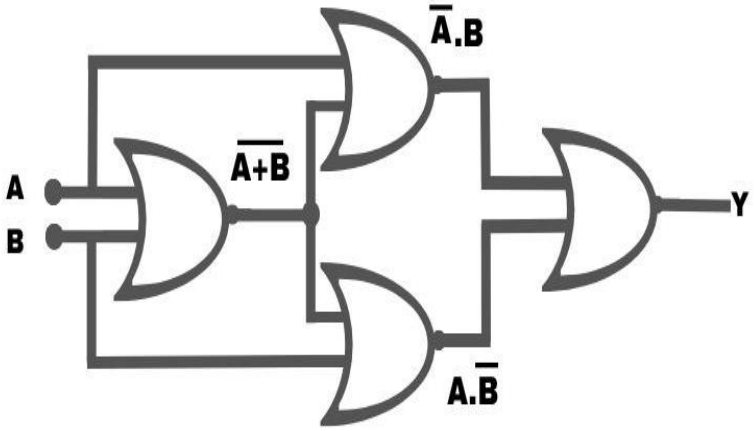


Truth Table

B (Input)	B (Input 2)	Y = A ⊕ B
0	0	0
0	1	1
1	0	1
1	1	0

XOR Gate using NOR Gate:

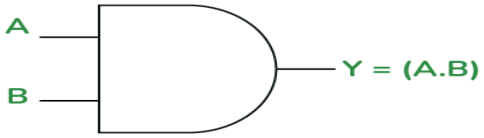
The following is the Implementation of XOR Gate using NOR Gate.



AND Gate Realization using NOR Gate:

AND gate is the fundamental logic gate that executes the logical multiplication of binary input. When all the inputs are 1, the AND Gate outputs 1, otherwise it outputs 0. A dot (.) denotes the AND operation.

AND Gate

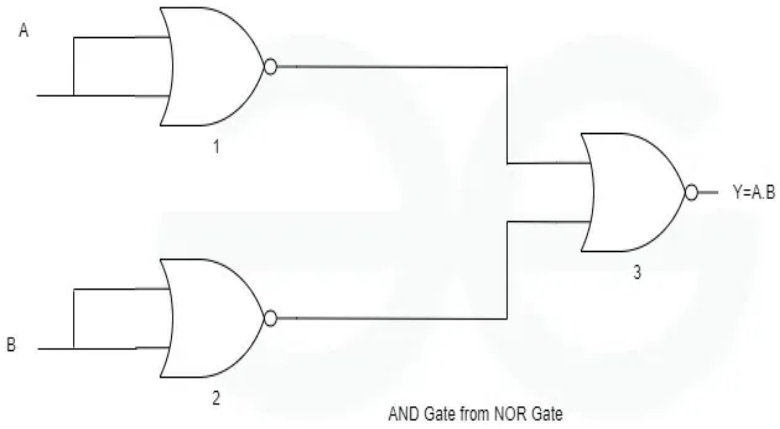


Truth Table

A (Input 1)	B (Input 2)	Y = (A.B)
0	0	0
0	1	0
1	0	0
1	1	1

AND Gate using NOR Gate:

The following is the Implementation of XOR Gate using NOR Gate.

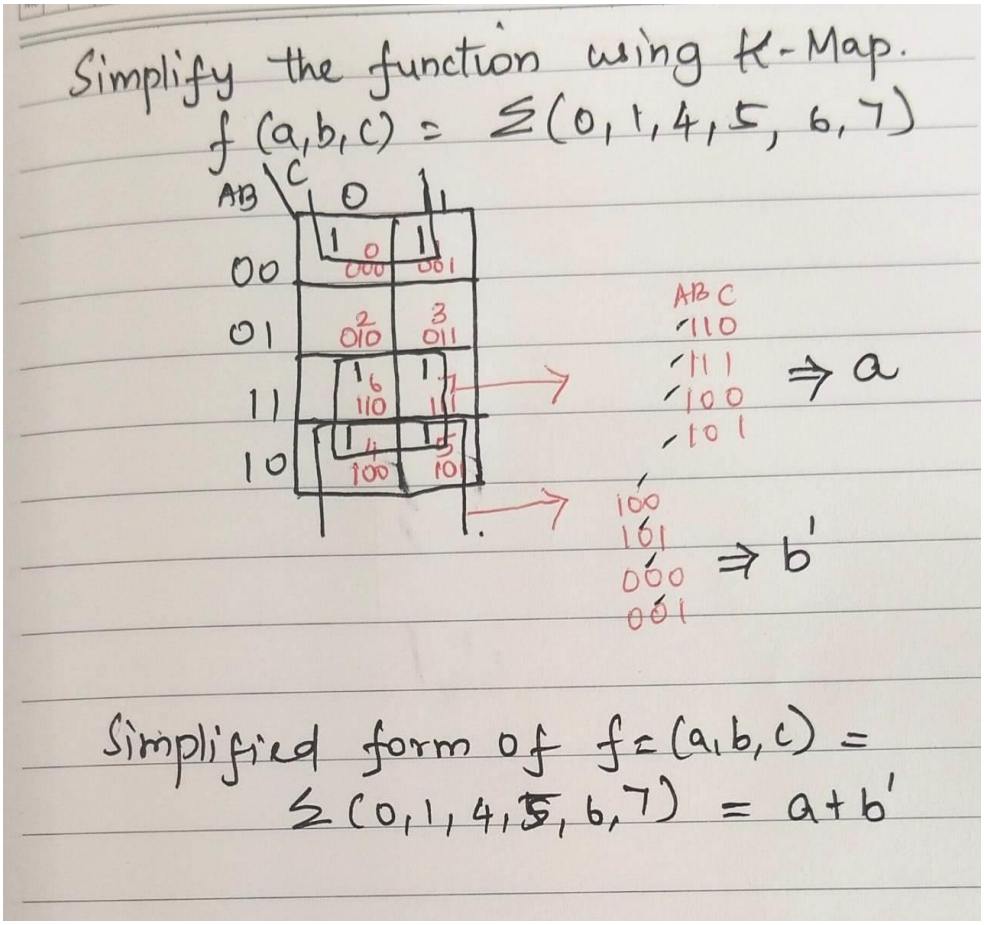


AND Gate from NOR Gate

2 (a) Simplify the following Function using K-Map:

f (a,b,c) = (0,1,4,5,6,7).

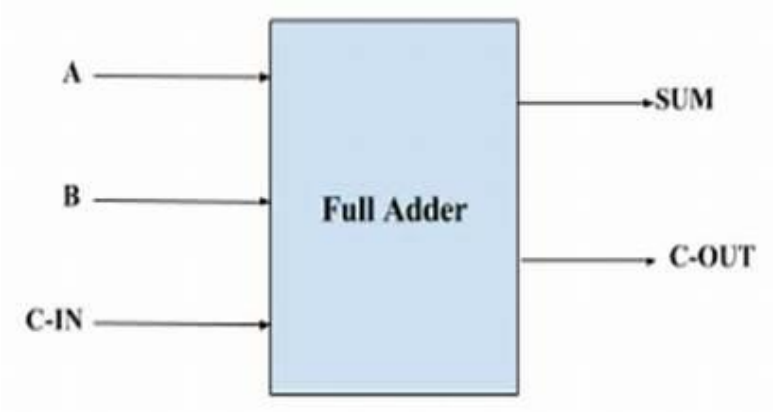
Correct K Map: 3 Marks
Correct Minterms: 3 Marks
Correct Grouping and Simplification: 4 Marks



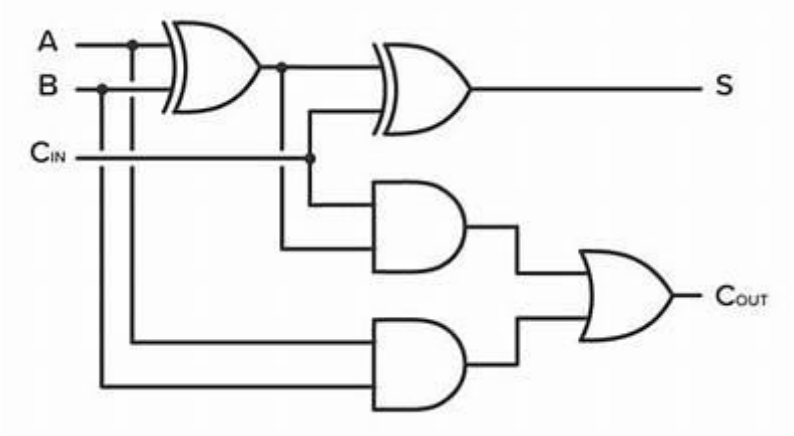
2 (b) Explain Full Adder with Circuit Diagram.

Full Adder is the adder that adds three inputs and produces two outputs. The first two inputs are A and B and the third input is an input carry as C-IN. The output carry is designated as C-OUT and the normal output is designated as S which is SUM. The C-OUT is also known as the majority 1's detector, whose output goes high when more than one input is high. A full adder logic is designed in such a manner that can take eight inputs together to create a byte-wide adder and cascade the carry bit from one adder to another. A full adder is used because when a carry-in bit is available, another 1-bit adder must be used since a 1-bit half-adder does not take a carry-in bit. A 1-bit full adder adds three operands and generates 2-bit results.

Block Diagram of a Full Adder:



Circuit Diagram of a Full Adder:



SUM = C-IN XOR (A XOR B)

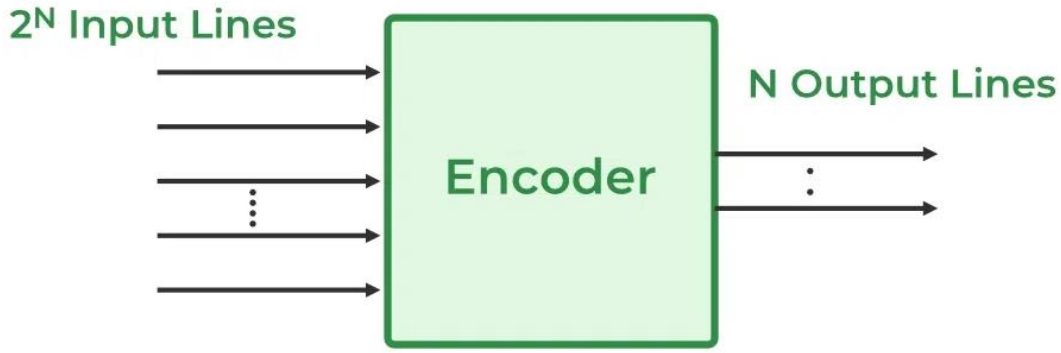
C_{OUT} = A B + B C_{IN} + A C $_{IN}$ = AB + (A $\oplus$ B).Cin

Explanation 3 Marks; Block Diagram 2 Marks; Logic Diagram and Equations: 5 Marks

2 (C)Explain the Priority Encoder with its Circuit Diagram.

An encoder is a digital circuit that converts a set of binary inputs into a unique binary code. The binary code represents the position of the input and is used to identify the specific input that is active. It has a maximum of **2^n input lines** and **'n' output lines**, hence it encodes the information from 2^n inputs into an n-bit code. It will produce a binary code equivalent to the input, which is active High. Therefore, the encoder encodes 2^n input lines with 'n' bits.

2n to n Encoder Block Diagram:



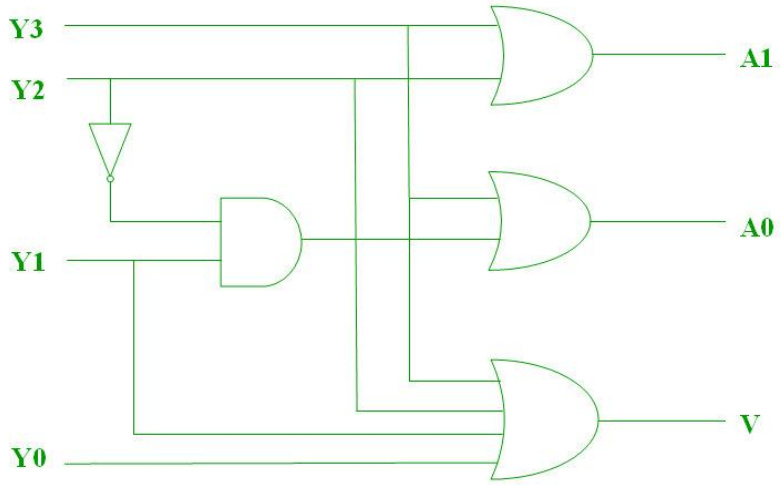
Priority Encoder

A 4 to 2 priority encoder has 4 inputs: Y3, Y2, Y1 & Y0, and 2 outputs: A1 & A0. Here, the input, Y3 has the highest priority, whereas the input, Y0 has the lowest priority. In this case, even if more than one input is '1' at the same time, the output will be the (binary) code corresponding to the input, which is having higher priority. The truth table for the priority encoder is as follows.

INPUTS				OUTPUTS		
Y3	**Y2**	**Y1**	**Y0**	**A1**	**A0**	**V**
0	0	0	0	X	X	0
0	0	0	1	0	0	1
0	0	1	X	0	1	1
0	1	X	X	1	0	1

INPUTS				OUTPUTS		
1	X	X	X	1	1	1

The Circuit Diagram of a Priority Encoder:



There are some errors that usually happen in Encoders are mentioned below.

- There is an ambiguity, when all outputs of the encoder are equal to zero.
- If more than one input is active High, then the encoder produces an output, which may not be the correct code.

So, to overcome these difficulties, we should assign priorities to each input of the encoder. Then, the output of the encoder will be the code corresponding to the active high inputs, which have higher priority.

Explanation 3 Marks; Block Diagram 2 Marks; Logic Diagram and Truth table: 5 Marks

2 (d) Write a note on Digital Comparator:

A digital combinational circuit used to compare the magnitude of two binary numbers to determine the equality or non-equality is called a comparator.

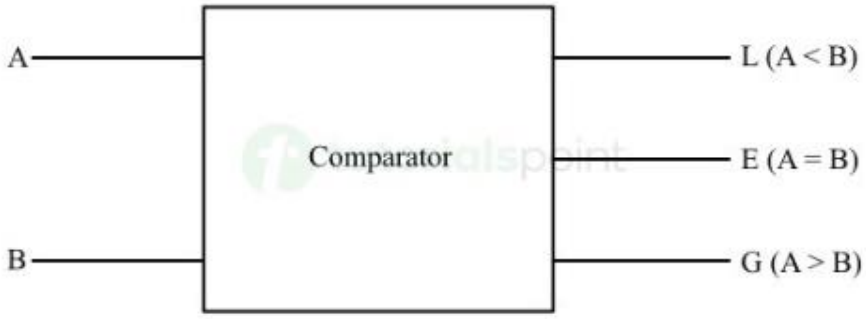
Therefore, the main function of a comparator is to compare the values of input numbers and produce an output indicating whether the numbers are equal or specifies which of the numbers is greater.

Let us understand the working of a comparator with the help of an example.

Consider two 3-bit binary numbers A2A1A0 and B2B1B0. These two binary numbers are said to be equal if all their corresponding bits coincide. In other words, these two binary numbers are equal if A2 = B2, A1 = B1, and A0 = B0.

Here, A and B are the input bits, and L, E, and G are the output lines, where L indicates which number is smaller, E indicates equality, and G indicates the greater number.

The block diagram of a typical comparator is shown in the following figure:



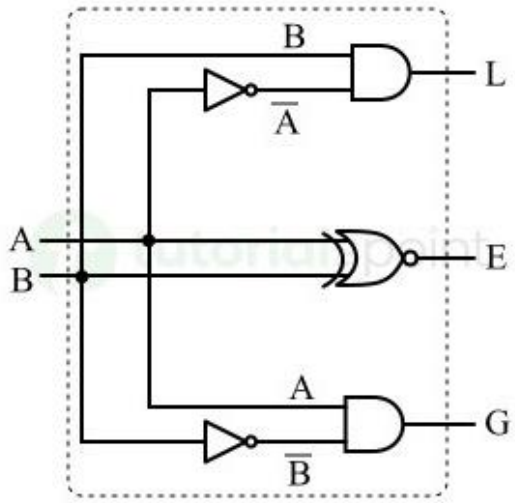
Depending on the number of bits, the following are some main types of comparators used in digital circuits –

- 1-Bit Magnitude Comparator
- 2-Bit Magnitude Comparator
- 4-Bit Magnitude Comparator

Inputs		**Outputs**		
A	**B**	**L (A < B)**	**E (A = B)**	**G (A > B)**
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

Explanation 3 Marks; Block Diagram 2 Marks; Logic Diagram and Truth table: 5 Marks

The logic circuit diagram of the 1-bit magnitude comparator is shown in the following figure.



3 (a) Discuss the Concept of Edge Triggering in Flipflops.

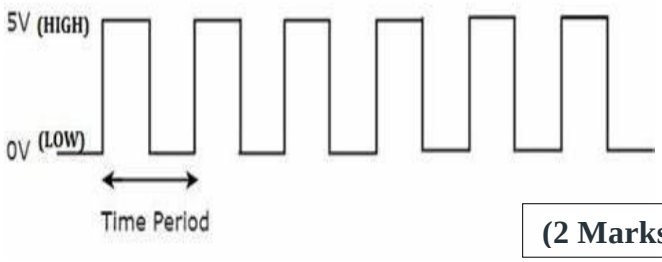
Edge Triggering:

In digital circuits, two methods of triggering are possible, namely edge triggering and level triggering, which trigger the signal to switch from one state to the other. Both form part of digital electronics and help in increasing throughput and controlling the timing of operations in a given system.

(2 Marks)

Clock Pulse:

A clock pulse represents a series of periodic pulses that control the time of operations in digital circuits. Synchronization is used in conjunction with sequential circuits as a clock signal to control the changing of states at certain instances. It is possible to use clock pulses to control other triggered devices such as flip- flop and counters because these elements should change their state only within certain time, for instance at the rising or falling edge of the pulse.

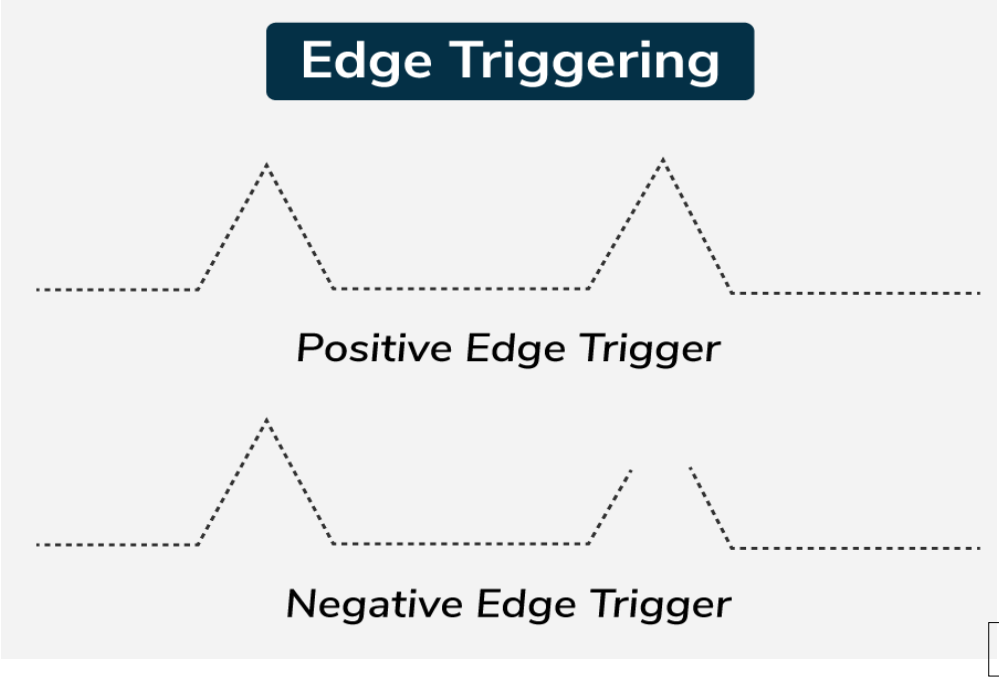


(2 Marks)

Edge Triggering:

It is used wherever it is required to identify the transition in the state of the input signal from low to high or from high to low. It is commonly applied to synchronous circuits, including flip-flops and counters. More often, edge triggering is advantageous when high accuracy of timing is required.

In edge triggering, the rapid change in the input signal that is sampled by the circuit's clock signal leads to a change in the signal. This edge, referred to as the trigger edge of the pulse, may be rising, that is, from a low state to high, or falling, that is, from high to low, depending on the circuit implementation. When the output signal crosses the trigger edge, the circuit changes the state of the output signal.



(3 Marks)

Advantages of Edge Triggering:

- Precise Timing: This simply ensures that the signal transition is correct and well timed due to timing needs such as flip-flops and counters.
- Reliability: Offers less chances of errors occurring due to noise or variance in the signal that is being received.

Disadvantages of Edge Triggering

- Complex Design: Demands stricter clock management, which leads to the augmentation of the resulting circuit complexity.
- High Sensitivity: May respond to unintended edges by noise, thus resulting in the possibility of an error in computation.

(3 Marks)

3 (b) Describe about Serial to Serial and Serial to Parallel Converter. **(5 Marks each)**

Serial to Serial Converter:

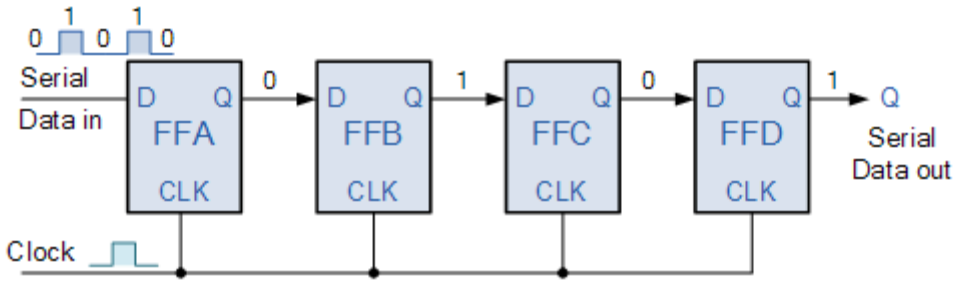
The Shift Register: The Shift Register is another type of sequential logic circuit that can be used for the storage or the transfer of binary data. A shift register basically consists of several single bit "D-Type Data Latches", one for each data bit, either a logic "0" or a "1", connected together in a serial type daisy-chain arrangement so that the output from one data latch becomes the input of the next latch and so on. Shift register IC's are generally provided with a clear or reset connection so that they can be "SET" or "RESET" as required. Shift registers operate in one of four different modes with the basic movement of data:

i. Serial-in to Parallel-out (SIPO)
ii. Serial-in to Serial-out (SISO)
iii. Parallel-in to Serial-out (PISO)
iv. Parallel-in to Parallel-out (PIPO)

Serial-in to Serial-out (SISO) – Serial to Serial Converter:

In Serial to Serial converter, the data is allowed to flow straight through the register and out of the other end. Since there is only one output, the DATA leaves the shift register one bit at a time in a serial pattern. It has only three connections, the serial input (SI) which determines what enters the left hand flip-flop, the serial output (SO) which is taken from the output of the right hand flip-flop and the sequencing clock signal (Clk). The logic circuit of a Serial to Serial converter:

4 Bit Serial to Serial Converter



This converter also acts as a temporary storage device or it can act as a time delay device for the data, with the amount of time delay being controlled by the number of stages in the register, 4, 8, 16 etc or by varying the application of the clock pulses.

Serial to Parallel Converter:

Assume that all the flip-flops (FFA to FFD) have just been RESET (CLEAR input) and that all the outputs QA to QD are at logic level "0" ie, no parallel data output.

If a logic "1" is connected to the DATA input pin of FFA then on the first clock pulse the output of FFA and therefore the resulting QA will be set HIGH to logic "1" with all the other outputs still remaining LOW at logic "0". Assume now that the DATA input pin of FFA has returned LOW again to logic "0" giving us one data pulse or 0-1-0.

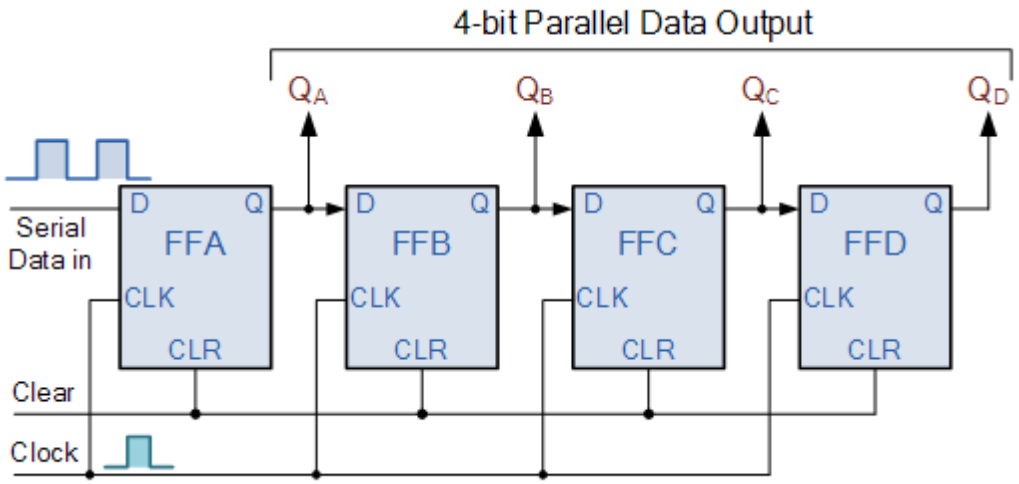
The second clock pulse will change the output of FFA to logic "0" and the output of FFB and QB HIGH to logic "1" as its input D has the logic "1" level on it from QA. The logic "1" has now moved or been "shifted" one place along the register to the right as it is now at QA.

When the third clock pulse arrives this logic "1" value moves to the output of FFC (QC) and so on until the arrival of the fifth clock pulse which sets all the outputs QA to QD back again to logic level "0" because the input to FFA has remained constant at logic level "0".

The effect of each clock pulse is to shift the data contents of each stage one place to the right, and this is shown in the following table until the complete data value of 0-0-0-1 is stored in the register. This data value can now be read directly from the outputs of QA to QD.

Then the data has been converted from a serial data input signal to a parallel data output. The truth table and following waveforms show the propagation of the logic "1" through the register from left to right as follows.

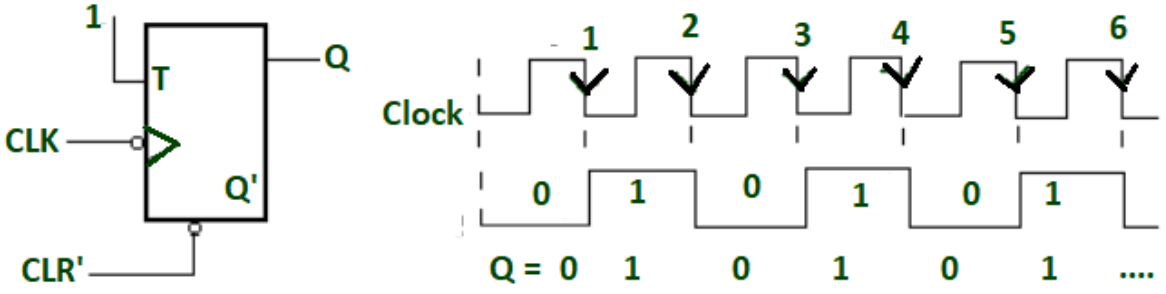
4 Bit Serial to Serial Converter



3 (c) Explain about Asynchronous UpCounter.

Asynchronous counters are a kind of digital circuitry which may count either upwards or downwards while not adhering to the timing pulses from an oscillator. As a result, state transitions are determined by extra inputs rather than by time frames at fixed intervals. The flip-flops and logic gates are utilized for designing the asynchronous counter in order to get counting sequence control based on input signals. With such characteristics they offer flexibility in counting and can be applied in many situations that demands am asynchronous action.

In asynchronous/ripple counter output of the first flip-flop is provided as the clock to the second flip-flop **i.e.,** flip-flop(FF) are not clocked simultaneously.



1 bit asynchronous/ripple counter

When two FFs are connected in series and output of one FF is act as clock for 2nd FF. So the state of 2nd FF will change only when output and 1st FF is logic 1 and falling edge occur. The output frequency of Q1 is f/4(if f is clock frequency).

It can generate 4 different unique states. This is known as divide by 4 circuits or mod 4 ripple counter. Here output is taken as Q1 (MSB) Q0(LSB). The Truth Table is as follows:

Y = Q when M= 0
Y = Q' when M=1

M	Q	Q'	Y
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

Working Procedure:

i. **Initialization**: The counter starts at 0 when powered on or reset.

ii. **Counting Mechanism**:

- The first flip-flop (FFA) is triggered directly by the clock pulse.
- For each clock pulse, FFA toggles its output (from 0 to 1 or 1 to 0).
- The output of FFA serves as the clock input for the next flip-flop (FFB). When FFA changes state, it triggers FFB.
- This ripple effect continues to the subsequent flip-flops (FFC, FFD, etc.), causing them to toggle in response to the changes in their preceding flip-flops.

iii. **Count Sequence**:

The counting proceeds in binary. For example:

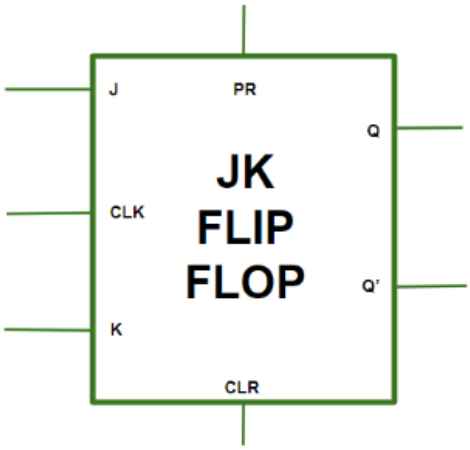
- 0 (0000)
- 1 (0001)
- 2 (0010)
- 3 (0011)
- 4 (0100)
- and so on...

Explanation 3 Marks; Block Diagram 2 Marks; Working Procedure and Truth table: 5 Marks

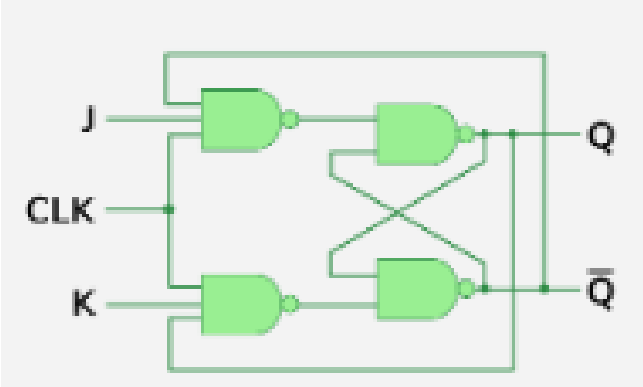
3 (d) Explain JK and D Flipflops. **(5 Marks each)**

Flip-flops are widely used for handling binary information. A Flipflop contains two statess- Set (S) and Reset (R). It consists of two inputs and two outputs. Inputs are Set(J) & Reset(K) and their corresponding outputs are Q and Q'. JK flipflop has two modes of operation which are synchronous mode and asynchronous mode. In synchronous mode, the state will be changed with the clock (clk) signal, and in asynchronous mode, the change of state is independent from its clock signal.

Block Diagram of JK Flipflop



Two 3-input NAND gates are used in place of the original two 2-input AND gates. The Logic Diagram is shown below:



The outputs at Q and Q' are coupled to each gate's third input. Since the two inputs are now interlocked, the SR flip-flop's cross-coupling enables the previously invalid condition of (S = "1", R = "1") to be employed to perform the "toggle action".

Truth table

J	K	Q_N	Q_{N+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

D Flipflop:

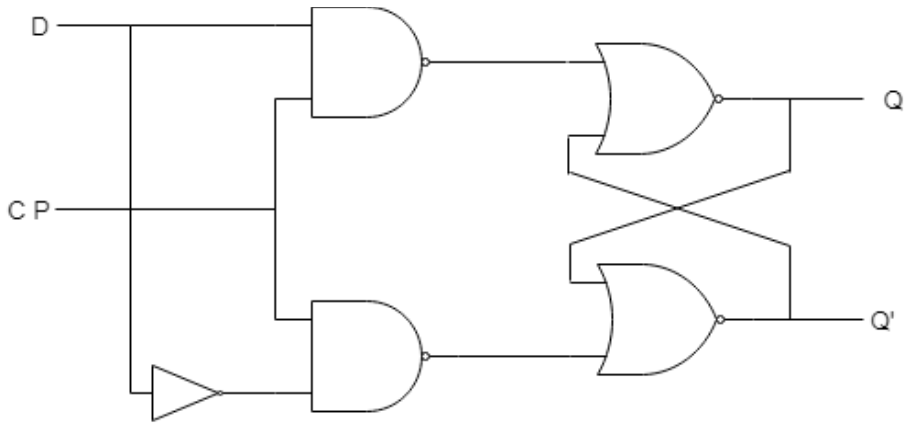
D flip flop is an electronic devices that is known as "delay flip flop" or "data flip flop" which is used to store single bit of data.D flip flops are synchronous or asynchronous. The clock single required for the synchronous version of D flip flops but not for the asynchronous one.The D flip flop has two inputs, data and clock input which controls the flip flop. when clock input is high, the data is transferred to the output of the flip flop and when the clock input is low, the output of the flip flop is held in its previous state.

Block Diagram of D Flipflop

D flip flop consist of a single input D and two outputs (Q and Q'). The basic working of D Flip Flop is as follows:

- When the clock signal is low, the flip flop holds its current state and ignores the D input.
- When the clock signal is high, the flip flop samples and stores D input.
- The value that was previously fed into the D input is reflected at the flip flop's Q output.
  - If D = 0 then Q will be 0.
  - If D = 1 then Q will be 1.
- The Q' output of the flip flop is complemented by the Q output.
  - If Q = 0 then Q' will be 1.
  - If Q = 1 then Q' will be 0.

The Logic Diagram is shown below:



Operation of D Flipflop:

- D is the input, and Q is current state, Qn + 1 is the next state outputs.
- Qn+1 will always be zero when D is 0, irrespective of current state of flip flop.
- When the input of the flip flop is 1, next state of flip flop will always be 1, regardless of the current state of flip flop.

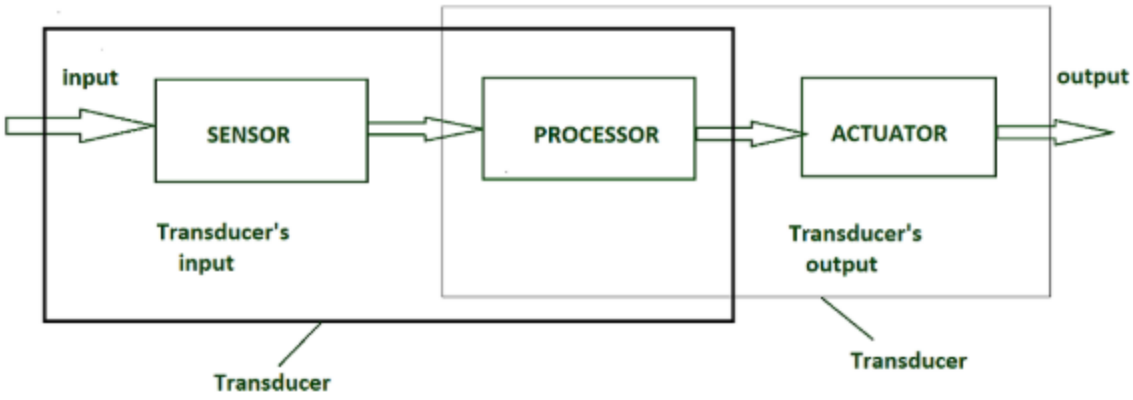
Truth Table

D	Q(Current)	Q(n+1) (Next)
0	0	0
0	1	0
1	0	1
1	1	1

4. (a) Describe about sensors and its types.

Sensors:

A Sensor is a characteristic of any device or material to detect the presence of a particular physical quantity. The output of the sensor is a signal, which is converted to human readable form. They detect and response to changes in the environment. These changes can be in form of light, temperature, motion, moisture or any other physical property. The sensor converts these physical changes into signal that can be measured.



Operation of a Sensor:

Transducer converts the signal from one physical form to another physical form. It is also called energy converter. For example, microphone converts sound to electrical signal. The processor processes the Electrical Signal. The processor is also programmed to perform certain functions for each value or range of values of the Transducer Output. The Actuator is activated by the Processor according to the programmed output series. **(5 Marks)**

Types of Sensors are listed below:

- Infrared Sensor(IR Sensor)
- Temperature & Thermocouple Sensors
- Proximity Sensor

- Ultrasonic sensor
- Accelerometers & Gyroscope Sensor
- Pressure Sensor
- Hall Effect Sensor
- Light Sensor
- Color Sensor
- Touch Sensor
- Tilt Sensor
- PIR Motion Detector & Vibration Sensor
- Metal detector, Water Flow & Heartbeat Sensor
- Flow and Level Sensor
- Smoke, Fog, Gas, Ethanol & Alcohol Sensor
- Humidity, Soil Moisture & Rain Sensor

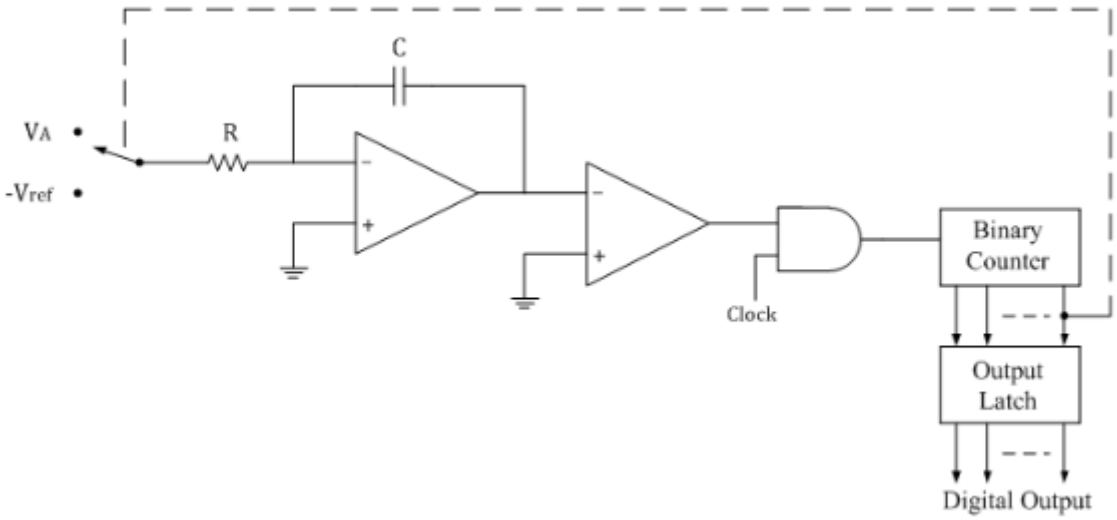
(5 Marks)

These sensors are used to detect and measure the appropriate factors. Ex: Ultrasonic and IR sensors are used in Vehicle Parking Systems. Light sensors are used in Human motion tracking system.

4. (b) Write about Dual Slope AD Converter:

Dual Slope Analog to Digital Converter:

In dual slope type ADC, the integrator generates two different ramps, one with the known analog input voltage VA and another with a known reference voltage –Vref.

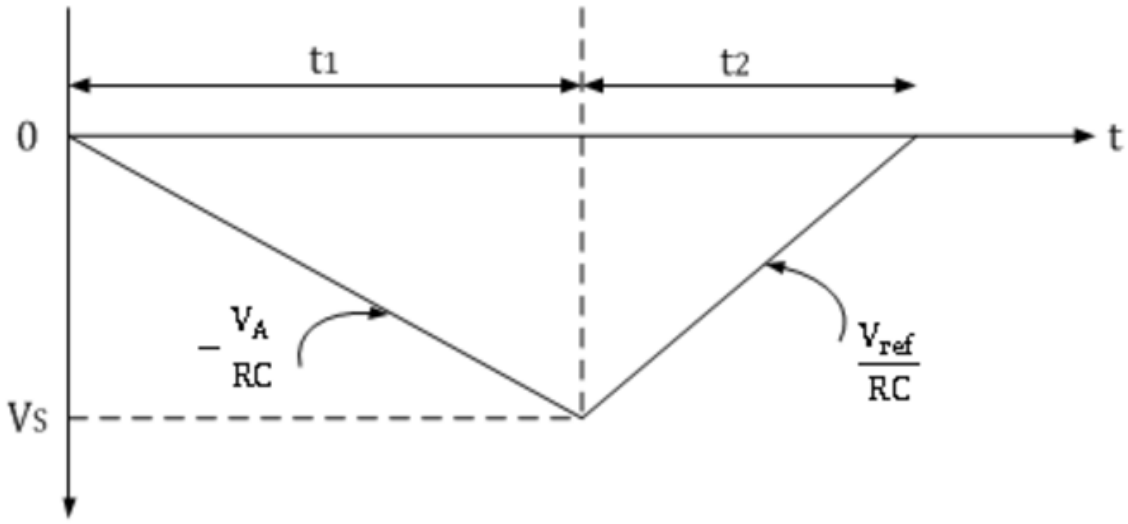


Operation:

The binary counter is initially reset to 0000; the output of integrator reset to 0V and the input to the ramp generator or integrator is switched to the unknown analog input voltage VA. The analog input voltage VA is integrated by the inverting integrator and generates a negative ramp output. The output of comparator is positive and the clock is passed through the AND gate.

Explanation and Logic Diagram: 5 Marks; Operation, Waveform and Equation: 5 Marks

The dual ramp output waveform



Since ramp generator voltage starts at 0V, decreasing down to –Vs and then increasing up to 0V, the amplitude of negative and positive ramp voltages can be equated as follows.

$$V_{ref}/RC \times t_2 = -VA/RC \times t_1$$
$$t_2 = -t_1 \times VA/V_{ref}$$
$$VA = -V_{ref} \times t_1/t_2$$

4. (c) Discuss about the weighted resistor D/A converter.

Binary weighted resistor digital to analog converter

A binary weighted resistor digital to analog converter (DAC) is a type of digital to analog converter that converts a digital input signal into an equivalent analog output signal by using a network of binary weighted resistors.

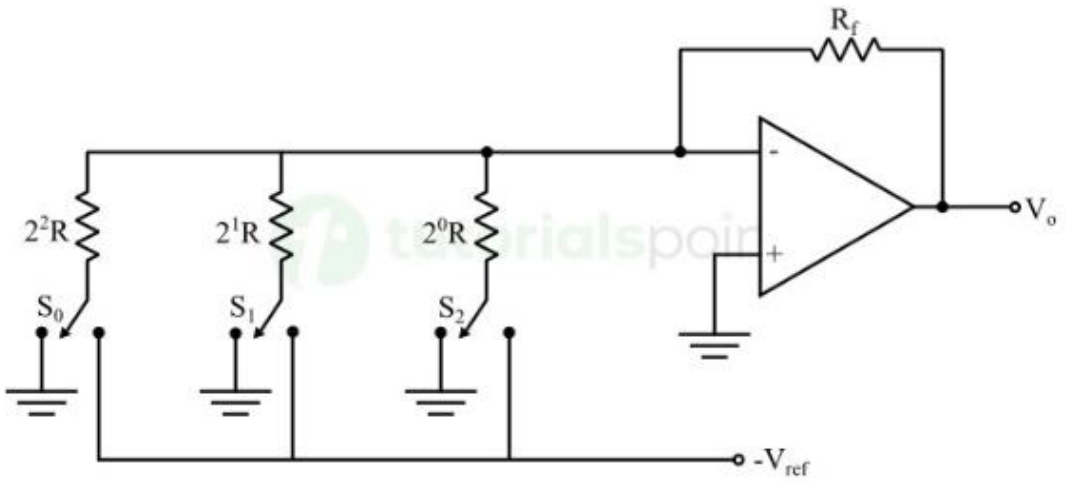
In simple words, a binary weighted resistor DAC uses a network of precision resistors with binary-weighted values to produce an analog output signal corresponding to the digital input signal.

The binary weighted resistor DAC utilizes a resistive ladder network connected to a summing amplifier to generate an analog output. In the ladder network, each resistor has a resistance value which is in a binary proportion to previous resistor.

It consists of a ladder network of binary weighted resistors connected to a summing amplifier (Op-Amp). Each resistor of the ladder network has a value weighted in binary proportion to the value of the preceding resistor. For example, if the value of first resistor is 20 R, i.e. R, then the value of the second resistor will be 21 R or 2R, similarly the value of third resistor is 22 R or 4R, and so on.

Explanation and Logic Diagram: 5 Marks; Operation: 5 Marks

Circuit diagram of a binary weighted resistor Digital to Analog Converter



The summing amplifier provided at the end of the ladder network sum up all the intermediate output values to generate an appropriate analog output signal.

Operation of a Weighted Resistor DAC:

Step 1 - Taking Digital Input

The binary weighted resistor DAC takes a digital input signal specified in the form of a group of bits. Each bit of the input signal has a binary weight, where the highest weight is associated with the MSB (Most Significant Bit) of the digital signal, while the lowest weight is associated with the LSB (Least Significant Bit).

Step 2 - Switching of Resistive Network

The digital input signal switches (connect or disconnect) resistors in the ladder network based on the bits of the signal. For example, a bit of the input signal has a binary weight of 21, i.e. 2 will connect the resistor with a value 2R in the ladder network.

Step 3 - Summing Amplifier & Analog Output

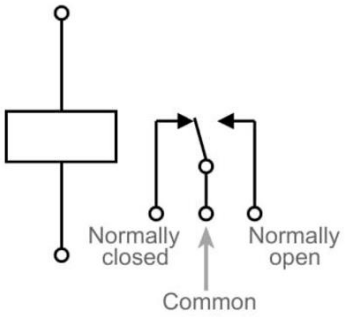
The summing or operational amplifier is connected at the summing node of the circuit. It combines different outputs of resistors together to produce a final analog signal at output.

4 (d) Write a note on relay and motor. **(5 Marks each)**

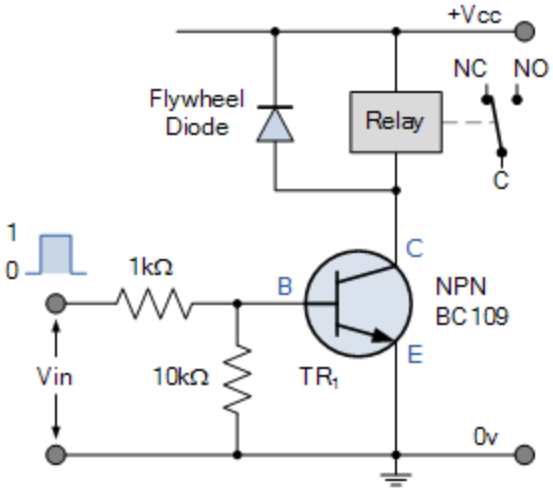
Relay Interfacing:

A relay is an electrically operated switch that uses an electromagnet to control the switching of a circuit. When a small current flows through the relay's coil, it generates a magnetic field that pulls a switch mechanism to open or close a separate circuit. Relays are used to control high-power devices with a low-power signal and can be found in many applications, including automotive systems and home appliances.

The symbol of a Relay is:



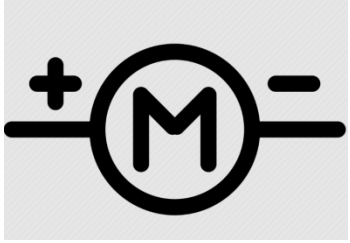
Electrical relays can be used to allow low power electronic or computer type circuits to switch relatively high currents or voltages both "ON" and "OFF". Some form of **relay switch circuit** is required to control it.



Motor Interfacing:

An electric motor is a device that converts electrical energy into mechanical motion. Understanding the basic concept of an electric motor is crucial before delving into the types and specific applications. Electric motors operate based on a fundamental principle of physics: electromagnetism. When an electric current flows through a conductor (such as a coil of wire), it generates a magnetic field.

The symbol of a Motor is:



4.6. Motor interfacing

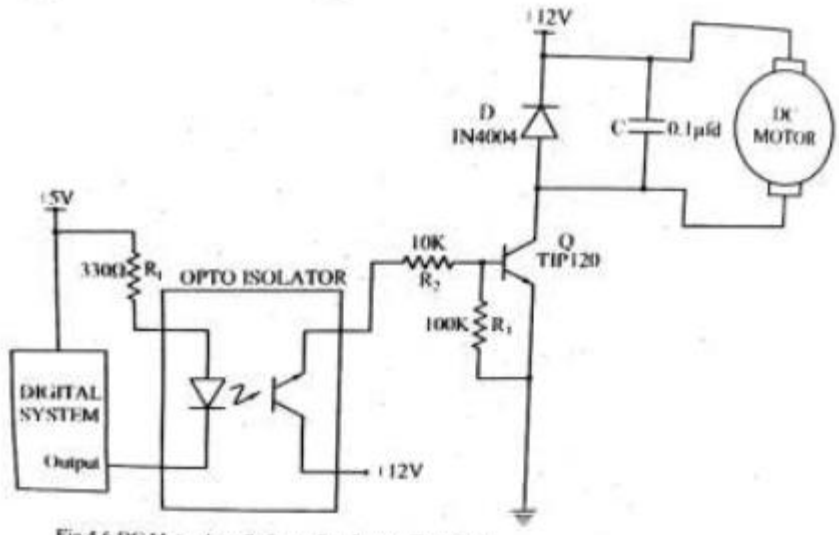


Fig.4.6.DC Motor Interfacing using Power Transistor

In Digital Electronics, Motors are used as Actuators for performing programmed output from a Sensor circuit. Ex: Stepper motors are used for performing SWITCH ON / OFF operation in a smoke detection sensor setup.

5 (a) Discuss about the classification of Read Only Memory (ROM). **(2 Marks each)**

ROM:

Read-Only Memory (ROM) is the primary memory unit of any computer system. Once data is stored, it remains within the unit, even when power is turned off and on again . The information is embedded in the ROM, in the form of bits, by a process known as programming the ROM .

Classification of ROM:

PROM:

It stands for Programmable Read-Only Memory. It is first prepared as blank memory, and then it is programmed to store the information. The difference between PROM and Mask ROM is that PROM is manufactured as blank memory and programmed after manufacturing. To program the PROM, a PROM programmer or PROM burner is used. Also, the data stored in it cannot be modified, so it is called as one – time programmable device.

Uses – They have several different applications, including cell phones, video game consoles, RFID tags, medical devices, and other electronics.

EPROM:

It stands for Electrically Erasable Programmable Read-Only Memory . It is similar to EPROM, except that in this, the EEPROM is returned to its initial state by application of an electrical signal, in place of ultraviolet light . Thus, it provides the ease of erasing, as this can be done, even if the memory is positioned in the computer. It erases or writes one byte of data at a time .

Uses – It is used for storing the computer system BIOS.

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Uses – It is used for storing the computer system BIOS.

Mask ROM:

Mask ROM is programmed during the manufacturing process, and the data cannot be changed once written.

Characteristics: Very cost-effective for large-scale production, but inflexible since the data is permanently fixed.

5(b) Describe about the operation of pen drive and solid state hard drive. **(5 Marks each)**

Pen Drive:

A pen drive also known as a USB flash drive, is a data storage device that includes flash memory with an integrated USB interface. A typical USB drive is removable, rewritable, and smaller than an optical disc, and usually weighs less than 30 g. A pen drive is a small yet powerful device that can help you transfer files between devices easily and quickly.

Operation of a Pen Drive:

- **Basic Components**: A USB drive consists of a USB connector, a flash memory chip, and a circuit board all enclosed in a protective casing. The USB connector enables the pen drive to connect with different devices, while the flash memory chip holds the data.
- **Mechanism for Storing Data:** Information is saved in the flash memory chip by means of electrical charges. This technique enables fast information access and retrieval, making pen drives highly effective.
- **Process of Transferring Data**: When you insert a USB flash drive into a USB port, it interacts with the operating system of your computer, enabling you to easily move files by dragging and dropping them. The easy-to-use nature of this process is a major factor driving the widespread use of pen drives.

Solid State Drive:

Solid-state drive (SSD) is a solid-state storage device that uses integrated circuit assemblies as memory to store data. SSD is also known as a solid-state disk although SSDs do not have physical disks. There are no moving mechanical components in SSD. This makes them different from conventional electromechanical drives such as Hard Disk Drives (HDDs) or floppy disks, which contain movable read/write heads and spinning disks. SSDs are typically more resistant to physical shock, run silently, and have quicker access time, and lower latency compared to electromechanical devices.

It is a type of **non-volatile** memory that retains data even when power is lost. SSDs may be constructed from random-access memory (RAM) for applications requiring fast access but not necessarily data persistence after power loss. Batteries can be employed as integrated power sources in such devices to retain data for a certain amount of time after external power is lost.

Operation of SSD:

Solid state drives (SSDs) use a combination of NAND flash memory technology and advanced controller algorithms. NAND flash memory is the primary storage component, divided into blocks and pages. An SSD contains a controller chip that manages data storage, retrieval, and optimization. The controller's major duties are wear leveling, which evenly distributes write and erase cycles to extend the SSD's lifespan which consolidates empty blocks to maintain optimal performance.

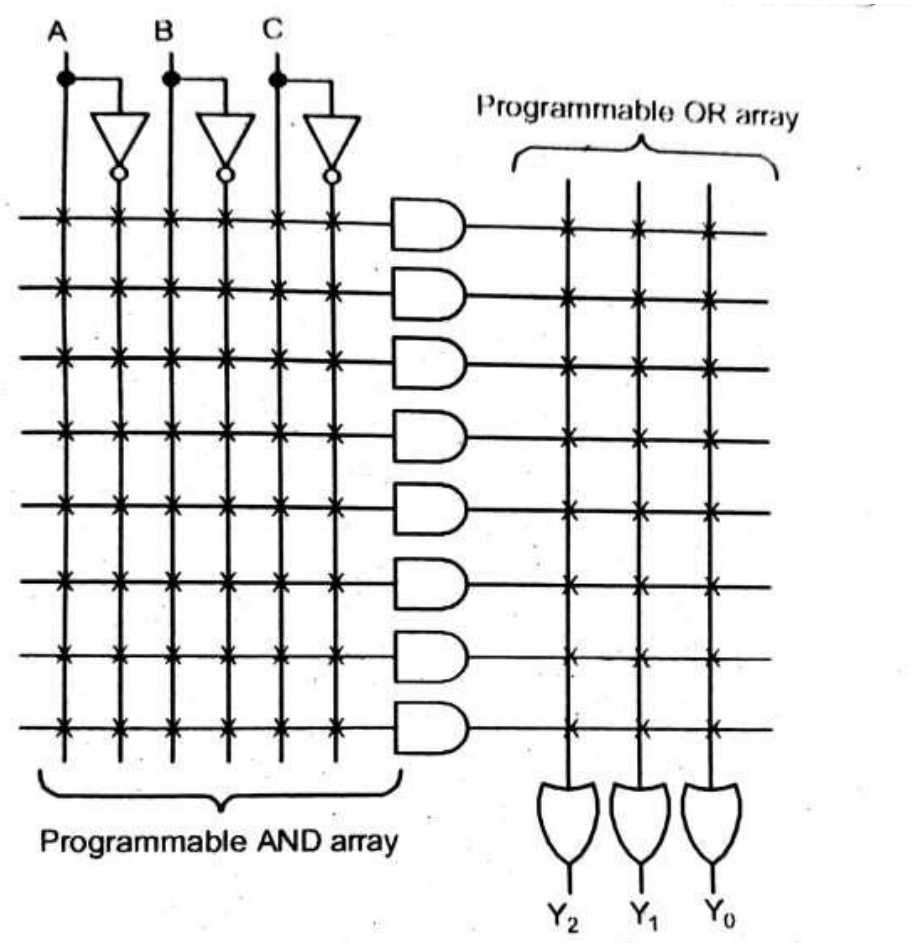
5(c) Describe about the PLA architecture with its diagram.

A Programmable Logic Array (PLA) is one of the simplest forms of programmable logic devices, made of a programmable AND array followed by a programmable OR array. PLA is a type of programmable logic device to construct a reconfigurable digital circuit on its architecture. It includes memory as well as logical operation which enable the user to instruct the device to perform certain operations of logic. PLAs are more versatile due to their capability of being programmed to operate multiple logic functions and hence can be used in the designing of specific hardware solutions.

Explanation: 3 Marks; Structure: 4 Marks; Operation: 3 Marks

Structure of PLA:

- **AND Array**: This is where inputs (or their complements) are fed into a matrix of AND gates. The AND gates create a combination of the input signals, forming product terms (minterms).
- **OR Array:** The outputs of the AND array are fed into a matrix of OR gates. The OR gates combine the product terms from the AND gates to form the output logic.
- **Output:** The output is derived by combining the product terms through the OR gates.



Operation:

- The input signals are passed through the programmable AND gates to create any possible combination of the input conditions.
- The outputs of the AND gates are fed into the OR gates, which can also be programmed to generate any logical function by summing the necessary product terms.
- Since both the AND and OR arrays are programmable, a wide variety of logic functions can be implemented.

5 (d) Write a note on memory accessing, hierarchy and management. **(3 Marks)**

Memory Accessing:

Memory accessing refers to the method by which the CPU or other hardware retrieves or writes data from/to memory. It involves the following processes:

1. Addressing: The CPU sends an address to the memory system to specify the exact location of data.

2. Memory Read/Write: The CPU issues either a read (to fetch data) or write (to store data) command.

3. Data Transfer: Based on the command, data is either read from the memory location and sent to the CPU or written into the memory location.

Memory access can be random (as in RAM, where any location can be accessed directly) or sequential (as in some storage devices like tapes, where data is accessed in a specific order).

Memory Processing: **(3 Marks)**

Memory processing refers to the way the memory and CPU interact to handle data storage and retrieval. The speed at which this occurs is critical for system performance. Key factors influencing memory processing include:

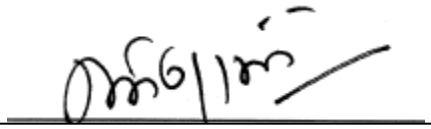
1. **Access Time:** The time it takes for the memory to respond to a request for data.
2. **Bandwidth:** The amount of data that can be transferred to and from memory in a given time period.
3. **Latency:** The delay between the initiation of a memory request and the actual data transfer.

Faster memory processing means quicker data transfer and more efficient system performance, often relying on advanced memory technologies such as caching and buffering to improve efficiency.

Memory Hierarchy: **(4 Marks)**

Memory like cache, and main memory are faster as compared to other types of memory but they are having a little less size and are also costly whereas some memory has a little higher storage value, but they are a little slower. Accessing of data is not similar in all types of memory, some have faster access whereas some have slower access.

1. **Registers**:
   - Fastest memory located within the CPU.
   - Extremely small in size, holds data temporarily for immediate CPU processing.
2. **Cache Memory**:
   - Faster than main memory but smaller.
   - Stores frequently accessed data to reduce access time.
3. **Primary Memory (RAM)**:
   - Volatile memory directly accessible by the CPU.
   - Larger than cache memory but slower.
4. **Secondary Storage (Hard Drives, SSDs)**:
   - Non-volatile memory used for long-term storage.
   - Slower than RAM but much larger in capacity.



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