

**DIPLOMA BOARD EXAMINATION – APRIL 2024**

**ANSWER KEY FOR THE QUESTION CODE – 684**

**SUBJECT CODE / NAME: 4052310 - BASICS OF ELECTRICAL AND  
ELECTRONICS ENGINEERING**

**BRANCH: CSE**

**SEMESTER: 3**

**MAXIMUM MARKS: 100**

- N.B 1. Answer all the questions under Part -A. Each questions carries 3 marks. (10x3=30)  
2. Answer all questions either (a) or (b) in Part-B. Each questions carries 14 marks.
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**PART - A**

- 1. State the difference between AC and DC current **3 Marks****

<b>Alternating current</b>	<b>Direct current</b>
Electron flow is bidirectional	Electron flow is unidirectional
AC signals are used in long transmission	DC signals are used in short transmission
AC signal changes their magnetic field	DC signal does not change its magnetic field
Alternating current varies with sinusoidally	Direct current remains in time steady state
AC signals can be stepped up. stepped down easily.	It is difficult to step up and step-down DC signal

- 2. Why do we need MCB? **3 Marks****

In order to protect low voltage electrical circuits from damage caused by excess current from an overload or short circuit we need an MCB. MCBs are used primarily as an alternative to the fuse switch.

- 3. Define current ratio of a transformer. **3 Marks****

It is the ratio of current flowing through the secondary to the current flowing through the primary winding.

For an ideal transformer,

$$V_1 = E_1 \text{ \& \ } V_2 = E_2$$

Input power = Output power

$$V_1 I_1 = V_2 I_2 \qquad \frac{V_2}{V_1} = \frac{I_1}{I_2}$$

Therefore,

$$\frac{E_2}{E_1} = \frac{I_1}{I_2} = K$$

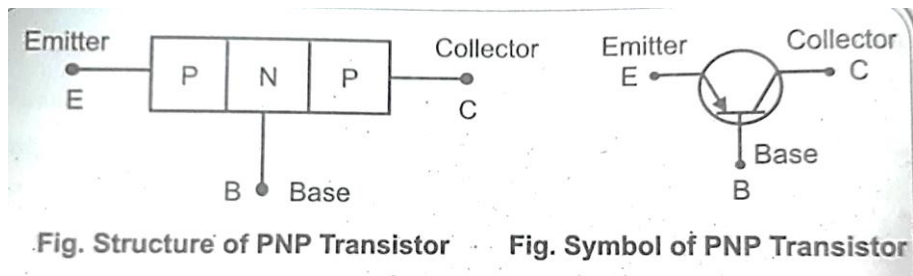
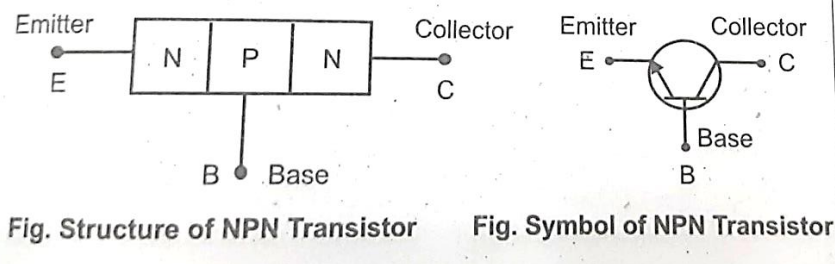
$$\text{Current ratio} = \frac{I_2}{I_1} = \frac{1}{K}$$

Hence current ratio is inverse of voltage transformation ratio.

**4. List the types of stepper motors** **3 Marks**

1. Permanent magnet stepper motor
2. Hybrid synchronous stepper motor
3. Variable reluctance stepper motor

**5. Draw transistor diagram.** **3 Marks**



**6. What are the NPN and PNP transistors?** **3 Marks**

In NPN transistor a P- type semiconductor is sandwiched between two N- type semiconductor.

In PNP transistor a N- type semiconductor is sandwiched between two P-type semiconductors.

**7. Convert the decimal number 9087 into an octal number.** **3 Marks**

$$(9087)_{10} = (21577)_8$$

		Remainders
8	9,087	7
8	1,135	7
8	141	5
8	17	1
8	2	2
	0	

↑

**8. Write any three Boolean laws****3 Marks****1. Commutative Laws**

It allows change in the position of variables in AND or OR expressions.

(i)  $A \cdot B = B \cdot A$

(ii)  $A + B = B + A$

**2 Associative Laws**

It allows removal of brackets from logical expression and regrouping of variables.

(i)  $A \cdot (B \cdot C) = (A \cdot B) \cdot C$

(ii)  $A + (B + C) = (A + B) + C$

**3. Distributive Laws**

It allows multiplying out of an expression.

(i)  $A \cdot (B + C) = (A \cdot B) + (A \cdot C)$

(ii)  $A + (B \cdot C) = (A + B) \cdot (A + C)$

**9. Distinguish between synchronous and asynchronous counter.****3 Marks**

Term	Asynchronous counter	Synchronous counter
Other name	It is also called as serial counter.	It is also called as parallel counter.
Trigger	Only the first FF is triggered by the external clock. The output first FF drives the clock of second FF and the output second FF drives the clock of third FF and so on. The flip flops are not triggered simultaneously.	All the flip flops are triggered by the same system clock signal simultaneously.
Speed	Operation speed is slow.	Operation speed is faster.
Design and implementation	Design and implementation are simple.	Design and implementation are complex.
Propagation delay	A subsequent propagation delay is encountered from one flip flop to another.	There is no propagation delay.
Decoding error	It produces decoding error.	It does not produce any decoding error.
Operation	It operates only in fixed count sequence (UP/ DOWN)	It operates in any desired count sequence

**10. List the applications of counter.**

**3 Marks**

- ✓ Count the number of times an event takes place.
- ✓ Frequency counters.
- ✓ Digital clocks.
- ✓ Analog to digital converters.
- ✓ Frequency divider.
- ✓ Used as Timers in electronic devices like ovens and washing machines.
- ✓ Digital Triangular Wave generator.

**PART – B**

**11. (a) Explain the construction of lead acid battery with neat sketch. (14 Marks)**

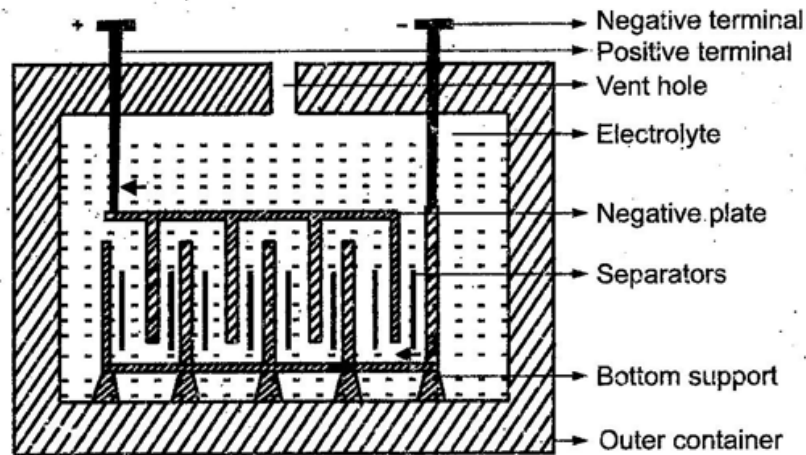
**(Diagram – 7 Marks, Explanation – 7 Marks)**

Battery is an electro - chemical device whose chemical reaction creates a flow of current in the circuit. It consists of two metal plates of different materials immersed in a suitable solution. The plates are called electrodes and the solution is called electrolyte.

**Construction of Lead Acid Cell**

Lead acid cell has a nominal cell voltage of 2V dc. It is commonly available in 6V and 12V batteries (3 or 6 cells connected in series) it is shown in figure. The lead acid cell consists of the following components.

1. Container
2. Plates
  - a. Positive plate
  - b. Negative plate
3. Electrolyte
4. Battery Terminals
5. Separators
6. Cell connectors
7. Cover of cell
8. Vent plug



**Lead acid battery**

### 1. Container

The battery container is constructed using either insulating or acid resistant material usually plastic or hard rubber and has a number of compartments or cells. At the bottom of the container, there are supports provided where the positive and negative plates rest.

### 2. Plates

In the batteries, the plates are of two types.

**(i) Positive plate:** It is made up of Lead peroxide ( $PbO_2$ ) deposited on a grid frame. The color of the positive plate is dark brown.

**(ii) Negative plate** It is made up of Spongy Lead ( $Pb$ ) deposited on a grid frame. The color of the negative plate is grey.

The grids are made up of an alloy of lead and antimony. The grid for the positive and negative plates are of the same design, but the grids for the negative plates are made lighter. The number of negative plates should be one higher than the number of positive plates.

### 3. Electrolyte

The battery is filled with electrolyte, which is a mixture of 35% sulfuric acid and 65% de-ionized water. The specific gravity of pure sulfuric acid is about 1.84 and this pure acid is diluted by distilled water until the specific gravity of the solution becomes 1.2 to 1.23 for longer life.

### 4. Battery terminals

A battery has two terminals; positive and negative. The terminals are made up of lead alloy.

(i) Positive pole shown '+' usually red in color and is the larger of the two.

(ii) Negative pole shown usually black or green and is the smaller of the two.

## 5. Separators

It separates the positive and negative plates from each other and prevents the short circuits. The separators must be porous so that the electrolyte may circulate between the plates. The separators must have higher insulating resistance and mechanical strength. The material used for separators are wood, rubber, glass, or pvc.

## 6. Cell connectors

It works like a link and used to connect the cells in series to get the desired voltage. All connections are made up of lead alloy. This is necessary to prevent galvanic corrosion.

## 7. Cover of cell

In lead acid battery the cover made up of the same material which is used for making container. It is used to cover the complete cell after the installation of the plates in it. It also protects the cell from the dust as well as other external impurities.

## 8. Vent plug

The vent plug is provided in the cover plate of the cell which is used to fill up the electrolyte in the cell or the inspection of internal condition of the cell. They are also used to exhaust the gases generated in the cell to the atmosphere.

## 11. (b) Explain the working principles of Online UPS with its block diagram.

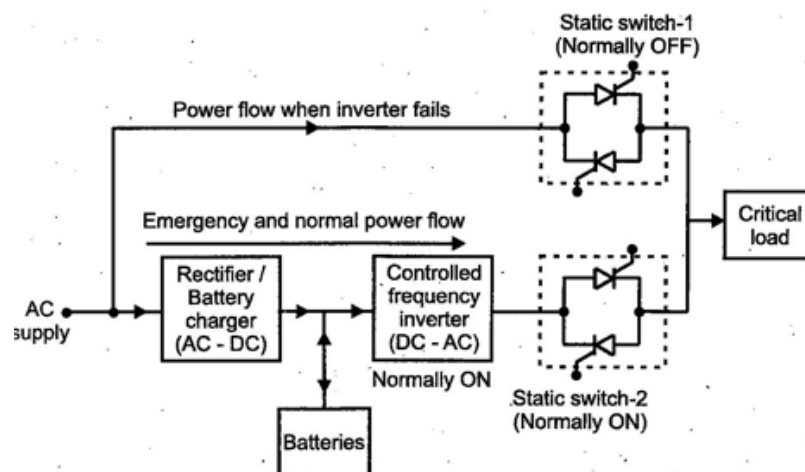
**(14 Marks)**

**(Diagram – 7 Marks, Explanation – 7 Marks)**

An Uninterruptible Power Supply (UPS) is defined as a piece of electrical equipment which can be used as an immediate power source to the connected load when there is any failure in the main input power source.

### **ON Line UPS (Inverter preferred UPS)**

The online UPS provides the highest and best level of power protection for critical applications. The block diagram of ON-Line UPS is shown in figure.



**Fig. Block diagram of ON Line UPS**

The major elements of online UPS are (i) Rectifier and Battery charger (ii) Inverter (iii) Static transfer switch (iv) Logic and control system (v) Battery bank.

## Operation

### Mode 1: Main ON

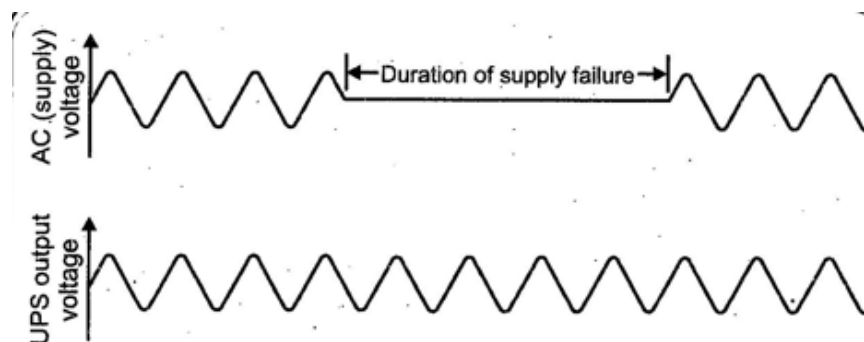
✓ During normal line conditions, the rectifier converts AC input supply to DC output. The rectifier provides power to the inverter. The inverter supplies energy to critical load through the static switch -2.

- ✓ The rectifier also charges the batteries continuously.
- ✓ The controlled frequency inverter will do the following functions.
  - Condition the supply to the load (converts DC to AC)
  - Protect the load from transients in the main supply
  - Maintain the load frequency at the desired value

### Mode 2: Main OFF

When the AC power supply fails, the inverter still supplies energy to the loads from the batteries.

As a consequence, no transfer time exists during the transition from normal to stored energy modes. The voltage waveform of ON-line UPS is shown in figure,



**Voltage waveform of AC supply and UPS**

### Mode 3: Over load

When an overload or inverter failure occurs, the bypass switch 1 connects the load directly to the AC mains, in order to guarantee the continuous supply of the load, thereby avoiding the damage to the UPS module (bypass operation)

Typical efficiency of the online UPS systems is up to 94%, which is limited due to the double conversion effect. Almost all commercial UPS units of 5 kVA and above are Online UPS Systems.

## Merits

- ✓ It provides full isolation of the critical load from the main AC supply.
- ✓ Since the inverter is always on, the quality of load voltage is free from distortion.
- ✓ Transfer time is practically zero as inverter is always on.

### Demerits

- ✓ Overall efficiency of the UPS is reduced.
- ✓ Cost is more.
- ✓ Battery life is low
- ✓ It consumes more power.

12. (a) Describe about the working principle of stepper motor with necessary diagram.

(14 Marks)

(Diagram – 7 Marks, Explanation – 7 Marks)

### Stepper Motor

A stepper motor is an electromechanical device which converts electrical pulses into discrete mechanical movement. The spindle of a stepper motor rotates in discrete step increments when electrical pulses are applied.

### Construction

The diagram of 3 phase 4 pole variable reluctance stepper motor is shown in figure.

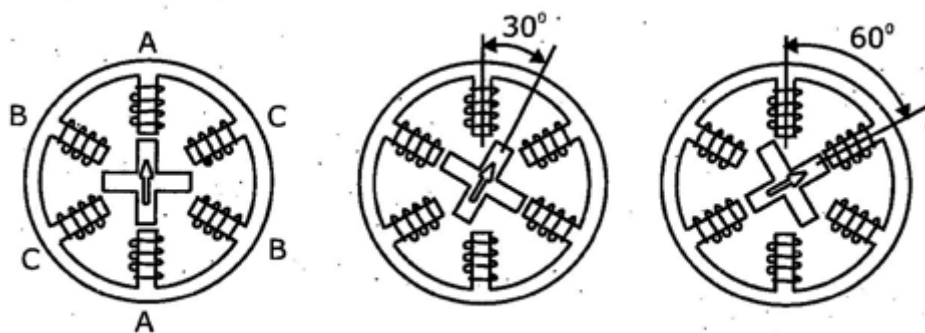


Fig. Stepper motor

A variable reluctance stepper motor has salient pole stator and rotor. The rotor is made up of soft iron with 4 pole and does not have any electrical winding. The stator has a stack of silicon steel laminations on which stator windings are wound. It has six equally spaced projecting stator poles for 3 phase winding. Diametrically opposite pairs of stator coils are connected in series, such that when one of them acts as N pole and the other acts as S pole. The number of stator and rotor poles depends on the required angular shift per pulse.

$$\text{Step angle} = \frac{360^\circ}{\text{umber of phases} \times \text{Number of rotor poles}}$$

### For a 3 phase 4 pole system

Number of phases = 3

Number of rotor poles = 4



$$\text{Step angle} = \frac{360^\circ}{3 \times 4} = 30^\circ$$

### **Working Principle**

When the stator windings are energized with DC current the poles become magnetized. Rotation occurs when the rotor teeth are attracted to the energized stator poles.

#### **Step 1**

When phase A is energized a magnetic field is created along the stator pole of phase A. The rotor teeth 1 and 3 line up with the axis A indicated by arrow.

#### **Step 2**

When phase A is switched off and phase B is energized a magnetic field is created along the stator pole of phase B. The rotor will move  $30^\circ$  clockwise to the new position indicated by arrow. The rotor teeth 2 and 4 line up with the axis of B.

#### **Step 3**

When phase B is switched off and phase C is energized a magnetic field is created along the stator pole of phase C. The rotor again will move  $30^\circ$  clockwise from the current position and the rotor teeth 1 and 3 line up with the axis C.

Hence by repetitively switching on the stator phases in the sequence ABCA the rotor will rotate clockwise in  $30^\circ$  steps. In our case it requires 12 pulses to complete one revolution. If the stator coils are excited in the order ACBA then motor will rotate in anticlockwise direction with the step size of  $30^\circ$ .

**12. (b) (i) Discuss the preventions and precautions against electric shock. (7 Marks)**  
**(Any 7 points)**

Human body is a conductor. If we touch a live wire, then the current passes through our human body and reaches the earth. Electric shock refers to the electricity passing through the human body, affecting the normal function of the heart, lungs and nervous system resulting in death.

To prevent electric shock it is always necessary to observe the following precautions.

1. Avoid contact with energized electrical circuits. Treat all electrical devices as if they are live or energized. Always be carefully.
2. Never touch any electrical equipment or circuits with wet hands.
3. Ensure that all electrical equipments are connected with good quality wires.
4. Ensure effective grounding and make sure that all the equipments are well grounded.
5. Always use insulated tools while working.

6. Use the special safety rubber gloves and rubber shoes.
7. Disconnect the power source before servicing or repairing electrical equipment.
8. Check all the wires and connectors for bad connections and signs of wear and defects. In case of defects replace cables instead of repairing with insulating tape.
9. Use plugs to connect the electric equipments to the switch board instead of bare wires.
10. Don't unplug the plug heads by pulling the wire.
11. Never overload circuits.
12. Install extra circuit protection devices, such as fuses, circuit breakers.

**12. (b) (ii) Write about the variable losses in transformer. (7 Marks)**  
**(Core or iron loss – 4 Marks, Copper loss – 3 Marks)**

The losses occurred in a static transformer are

1. Core or iron loss
2. Copperloss

**1. Core or Iron Loss**

Iron losses are caused by the alternating flux in the core of the transformer. It includes hysteresis and eddy current loss.

Total core losses Hysteresis loss + Eddy current loss

$$P_i = P_h + P_e$$

**(i) Hysteresis loss**

Power is dissipated in the form of heat known as hysteresis loss and given by the equation shown below. Hysteresis losses can be minimized by using silicon steel material for the construction of the core of the transformer.

$$P_h = K_h B_{max}^{1.6} fV \text{ Watts}$$

Where,  $K_h$  Hysteresis constant

f - Frequency

Bmax - Maximum or peak value of the flux density

V - Volume of the core

**(ii) Eddy current loss**

When the flux links with a closed circuit, an emf is induced in the circuit and the current flows. Since the core is made of conducting material, these EMFs circulates currents within the body of the material. These circulating currents are called Eddy Currents. The eddy current loss

is minimized by making the core with thin laminations. The equation of the eddy current loss is given as

$$P_e = K_e B_{max}^2 f^2 t^2 V \text{ Watts}$$

Where,  $K_e$  Eddy current constant.

$B_{max}$  - Maximum value of flux density in wb/m<sup>2</sup>

$T$  - Thickness of lamination in meters

$f$  - Frequency of reversal of magnetic field in Hz

$V$  - Volume of magnetic material in m<sup>3</sup>

The core loss is constant for all loads. So the core loss is also called as constant loss.

## 2. Copper Loss

These losses occur due to ohmic resistance of the transformer windings.

Total copper losses = Copper loss in primary winding + Copper loss in secondary winding

$$P_{cu} = I_1^2 R_1 + I_2^2 R_2 \quad \text{or} \quad I_1^2 R_{01} + I_2^2 R_{02}$$

Where,  $I_1$  Primary current

$I_2$  Secondary current

$R_1$  - Primary resistance

$R_2$  - Secondary resistance

These losses varied according to the load. Hence it is also known as **variable loss**.

So, Total losses in a transformer = Constant loss + Variable loss

$$= (P_h + P_e) + P_{cu}$$

$$\text{Total losses in a transformer} = P_i + P_{cu}$$

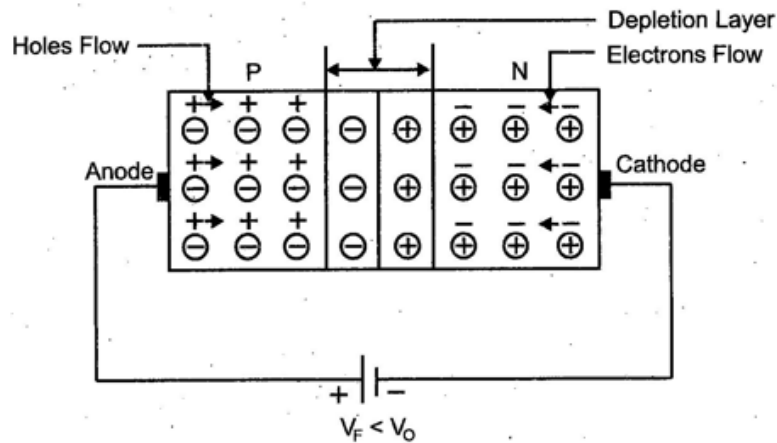
**13. (a) With the diagram explain the forward and Reverse characteristics of PN junction diode.**

**(14 Marks)**

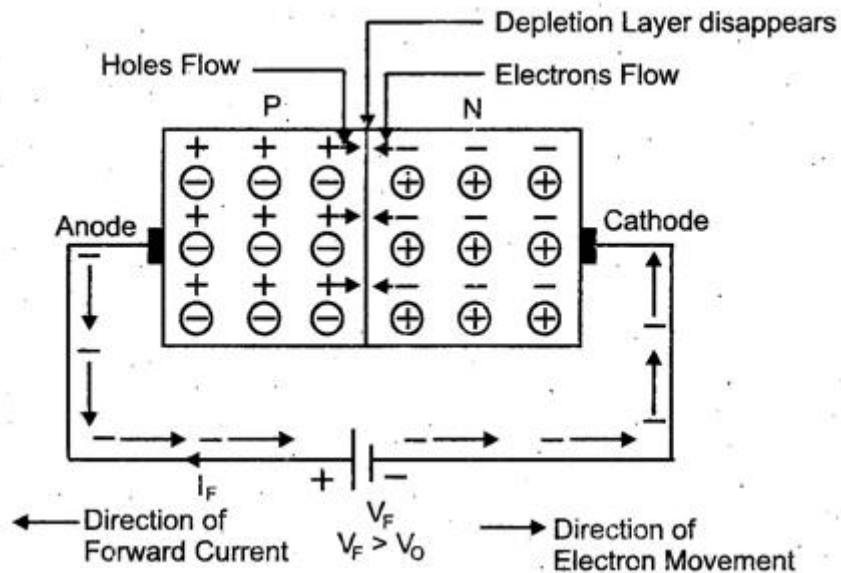
**(Forward biasing – 7 Marks, Reverse Biasing – 7 Marks)**

### (i) Forward Biasing

When positive terminal of the battery is connected to P- region and negative terminal of the battery is connected to N- region of the PN junction diode, the bias applied is known as forward bias.



**PN Junction forward biased**



**Direction of forward current**

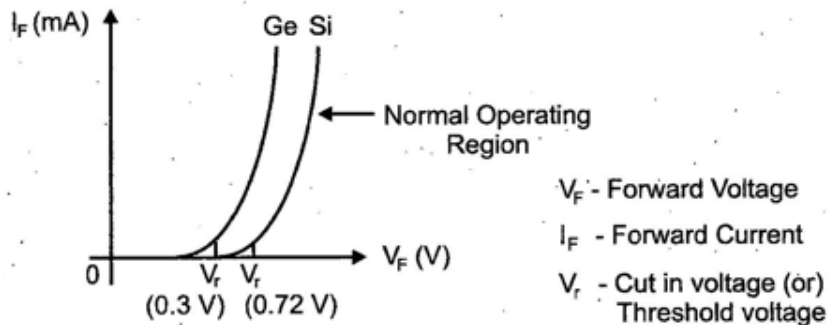
The voltage applied at the positive terminal repels the holes in P region. So, the holes move towards the junction. The voltage applied at the negative terminal repels the free electrons in the N-region. So, the free electrons move towards the junction.

**When  $V_F < V_0$ :** When the applied voltage is less than the potential barrier  $V_F < V_0$  the forward current is almost zero. Because the potential barrier prevents the movement of holes from P-region to N-region and the movement of free electrons from N-region to P-region.

**When  $V_F > V_0$**  When the applied voltage is greater than the potential barrier  $V_F > V_0$ , the depletion region and the barrier potential disappear. Hence the holes cross the junction from P- region to N-region and the electrons cross the junction from N- region to P-region. Hence a

large current flow in the circuit. The forward voltage at which the current through the junction starts to increase rapidly is known as cut in voltage (or) threshold voltage ( $V_t$ ) or knee voltage.

**Forward Bias Characteristics**



When  $V_F = 0$  When the forward voltage is Zero  $V_F = 0$  the forward current is zero  $I_F = 0$ . Because the potential barrier does not allow the current flow.

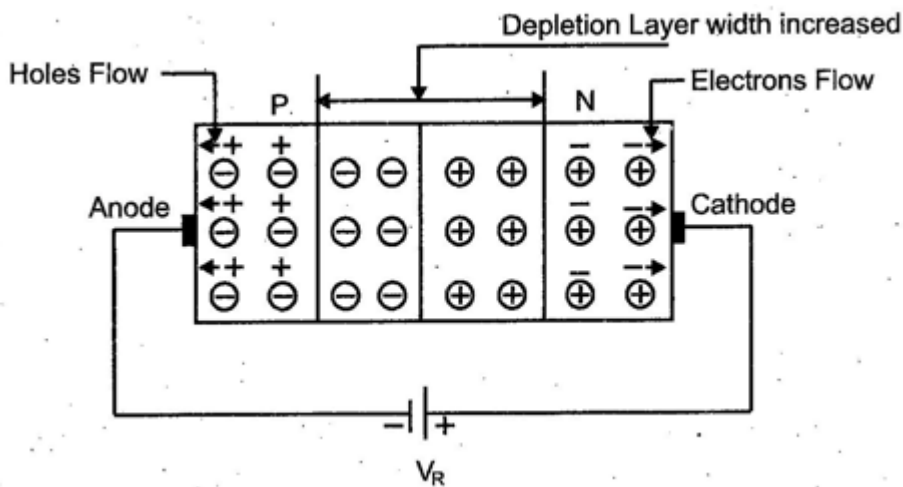
When  $V_F < V_0$  When the forward voltage is increased upto the barrier potential  $V_F < V_0$ , the current increases very slowly with increase in forward voltage  $V_F$

When  $V_F > V_0$ : When the forward voltage is greater than the barrier potential  $V_F > V_0$ , the current increases very sharply with increase in applied forward voltage  $V_F$  The cut in voltage for Germanium is 0.3 V and 0.72 V for Silicon.

**(ii) Reverse Biasing**

When the negative terminal of the battery is connected region and the positive terminal of the battery is to P connected to N-region the bias applied is known as reverse bias.

The positive terminal of the battery attracts the electrons in N region. So, the electrons move towards the positive terminal of the battery. The negative terminal of the battery attracts the holes in p - region. So, the holes move towards the negative terminal of the battery.



**PN Junction reverse biased**

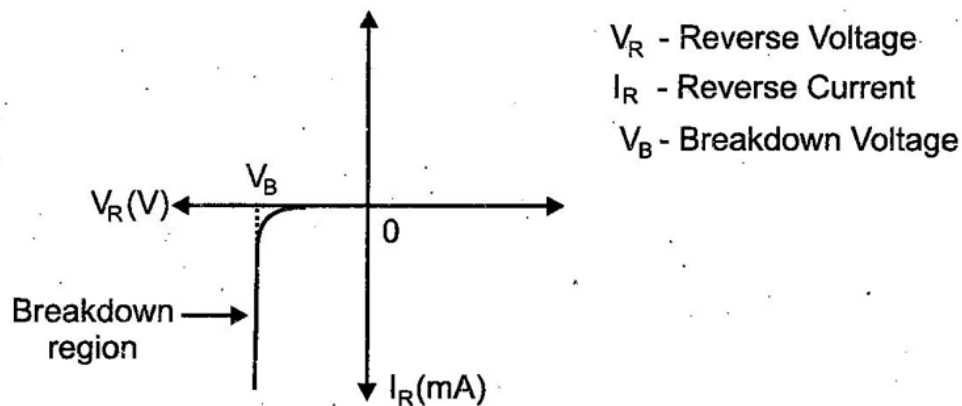
At reverse bias, the width of the depletion region increases. It results in increasing the potential barrier. It prevents the movement of electrons from N-region to P- region and holes from P-region to N-region. Therefore, no current flows. But practically, a small current flow in the circuit due to minority carriers. This current is known as reverse saturation current.

When the applied voltage is increased, beyond the saturation level, breakdown occurs. The reverse voltage at which the junction breakdown occurs is known as breakdown voltage ( $V$ ).

### Reverse Bias Characteristics

When the reverse voltage is applied, the width of the depletion region increases. No current flows through the circuit.

But practically a small amount of current flows in the circuit. This is called reverse saturation current ( $I_s$ ). This is due to minority carriers.

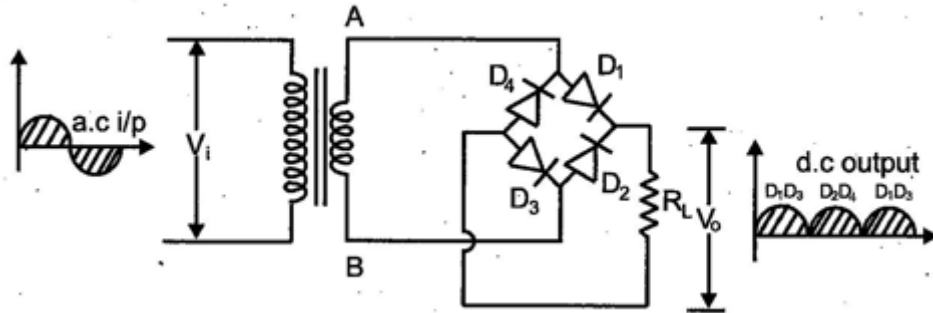


**Fig. Reverse Characteristics**

**13. (b) With the diagram explain the operation of Bridge rectifiers. (14 Marks)**

**(Diagram – 7 Marks, Explanation – 7 Marks)**

The bridge rectifier is a full wave rectifier. It contains four diodes  $D_1$ ,  $D_2$ ,  $D_3$  and  $D_4$ . They are connected to form a bridge. The ac input voltage is applied to one diagonal of the bridge through a transformer. The rectified dc voltage is taken from the other diagonal of the bridge. The load resistance  $R$ , is connected between the other two ends of the bridge. The need for center tapped transformer in a full wave rectifier is eliminated in the bridge rectifier.

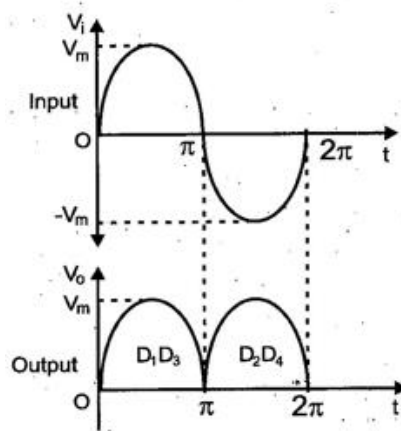


### Operation

**During the positive half cycle** of ac input voltage, terminal A becomes positive with respect to B. The diodes  $D_1$  and  $D_3$  are forward biased. The diodes  $D_2$  and  $D_4$  are reverse biased. The current flows from A to B through  $D_1$ ,  $R_L$ ,  $D_3$ . The diodes  $D_2$  and  $D_4$  do not conduct. So the whole input voltage appears across the load resistance  $R_L$ .

**During the negative half cycle** of ac input voltage, the terminal A becomes negative with respect to B. The diodes  $D_2$  and  $D_4$  are forward biased. The diodes  $D_1$  and  $D_3$  are reverse biased. The current flows from B to A through  $D_2$ ,  $R_L$ ,  $D_4$ . The diodes  $D_1$  and  $D_3$  do not conduct. So the whole input voltage appears across the load resistance  $R_L$ .

### Input and Output Waveforms



The load current is in the same direction for both half cycles of a. c input voltage. Hence d.c is obtained at the output.

### Advantages

- ✓ The center tap transformer is not required.
- ✓ It is cheaper.
- ✓ It reduces the losses.
- ✓ Transformer utilization factor is high.

### Disadvantages

- ✓ It requires four diodes.

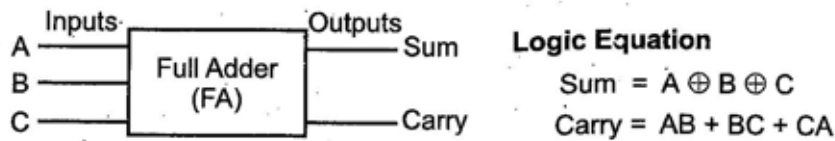
**14. (a) Explain the full adder and multiplexer with their diagrams and truth tables.**

**(14 Marks)**

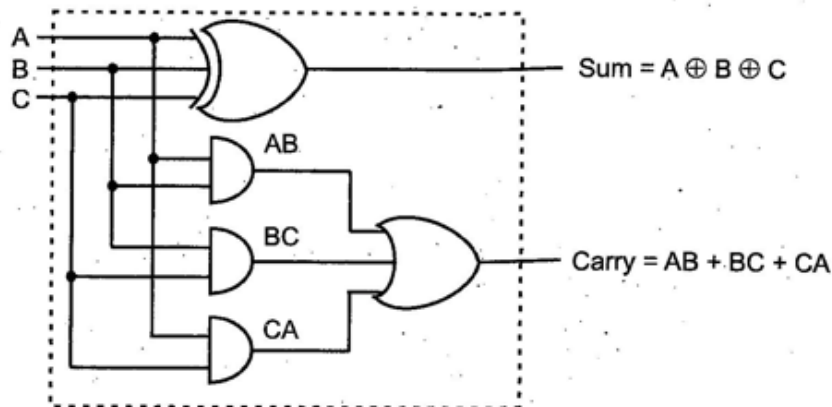
**(Full adder – 7 marks, Multiplexer – 7 Marks)**

**Full Adder:**

Full adder is a combinational logic circuit which is used to add three binary bits. It is a 3-bit adder. It has three inputs A, B, C and two outputs sum and carry. Two inputs A and B are the significant bits to be added. The third input C is the carry generated by the previous addition.



**Fig. Logic Symbol**



**Fig. Logic Diagram**

Inputs			Outputs	
A	B	C	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

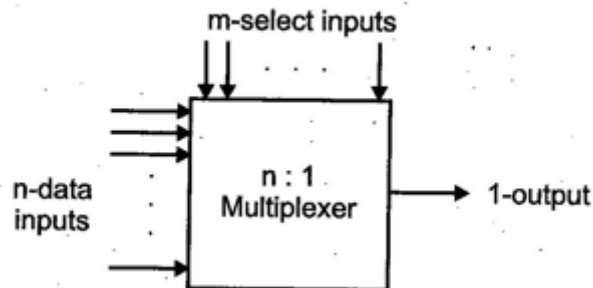
**Table. Truth Table**

A three input EX - OR gate is used to produce the sum. When three AND gate outputs are OR ed, it produces carry.



## Multiplexer:

Multiplexer means 'Many to one'. Multiplexer is a combinational logic circuit that places many inputs on a single output line as per the select inputs (control inputs). Depending upon the select line one of the data inputs is selected and passed to the output line. Hence it is also known as data selector.



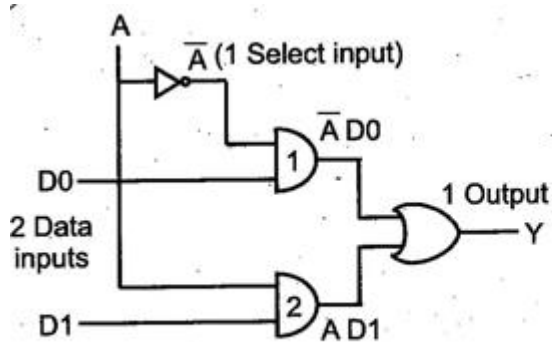
**Block Diagram of n: 1 multiplexer**

It has many inputs and only one output.. The number of select inputs depends on the number of data inputs. For an n- input multiplexer, m select inputs are required.

Where,  $n=2^m$

### **2-to-1 Multiplexer**

It has 2 data input lines D0, D1, one select line A and only one output Y



**Fig. Logic Diagram**

### **Logic Equation**

$$Y = \bar{A} D0 + A D1$$

Select Input A	Output Y
0	D0
1	D1

**Table. Truth Table**

Depending upon the select input, only one data input will be available at the output.

When  $A = 0$ , first AND gate is enabled. So the input D0 is selected.

When  $A = 1$ , second AND gate is enabled. So the input D1 is selected.

### 4-to-1 Multiplexer (4-input Multiplexer)

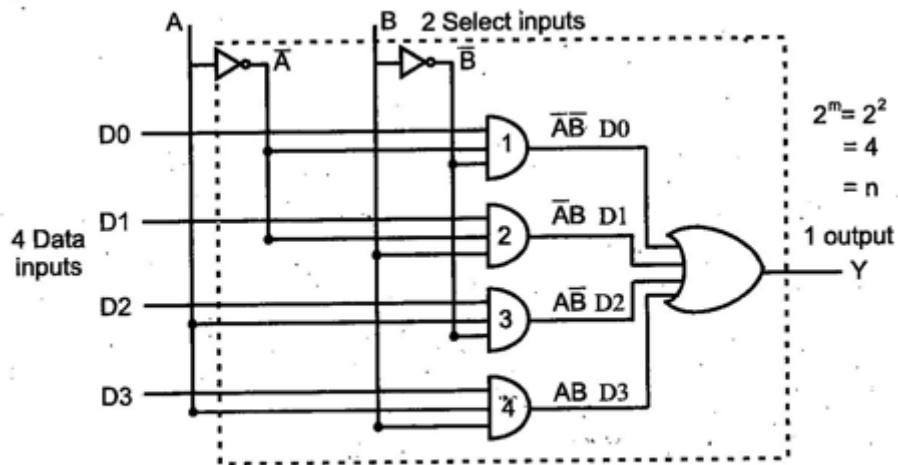


Fig. Logic Diagram of 4 : 1 Multiplexer

It has 4 input lines D0, D1, D2, D3 and two select inputs A, B and only one output Y

#### Logic Equation

$$Y = \bar{A}\bar{B}D_0 + \bar{A}BD_1 + A\bar{B}D_2 + ABD_3$$

Select Inputs		Output
A	B	Y
0	0	D0
0	1	D1
1	0	D2
1	1	D3

Table. Truth Table

Depending upon the select inputs, only one data input will be available at the output.

#### Example

When A = 0 and B = 1, the second AND gate is enabled. So the second data input D1 is selected. The output Y = D1.

**14. (b) Construct AND, OR, NOT, NOR and XOR gates using NAND gate along with truth tables. (14 Marks)**

**(AND gate – 2 Marks, OR gate – 2 Marks, NOT gate – 2 Marks, NOR gate – 4 Marks, NAND gate – 4 Marks)**

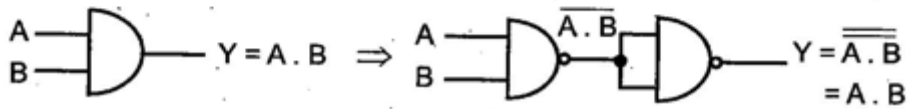
**AND gate using only NAND gates**

**Logic Equation**

$$Y = A \cdot B$$

$$= \overline{\overline{A \cdot B}} \quad (\because \overline{\overline{A}} = A \text{ laws of complementation})$$

**Logic Diagram**



**OR gate using only NAND gates**

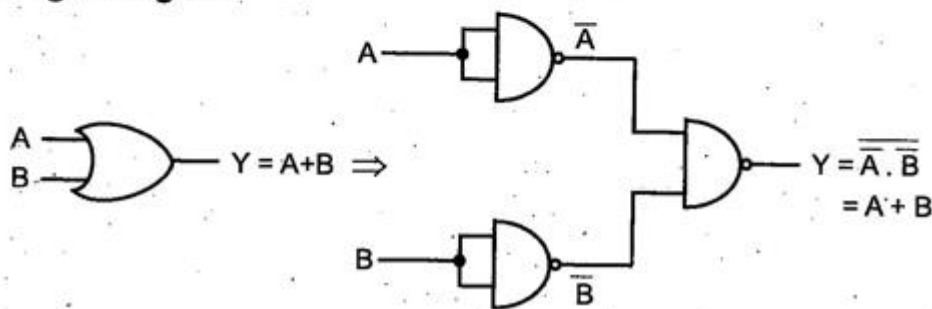
**Logic Equation**

$$Y = A + B$$

$$= \overline{\overline{A + B}} \quad (\because \overline{\overline{A}} = A \text{ laws of complementation})$$

$$= \overline{A \cdot B} \quad (\because \overline{A + B} = \overline{A} \cdot \overline{B} \text{ Demorgan's first theorem})$$

**Logic Diagram**



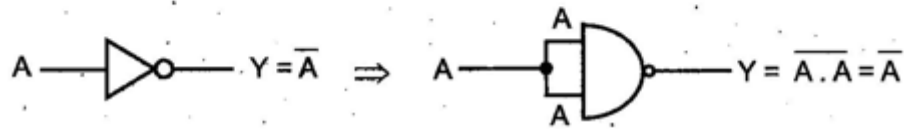
**NOT gate using only NAND gate**

**Logic Equation**

$$Y = \overline{A}$$

$$= \overline{A \cdot A} \quad (\because A = A \cdot A \Rightarrow \text{AND laws})$$

**Logic Diagram**



**NOR gate using only NAND gates**

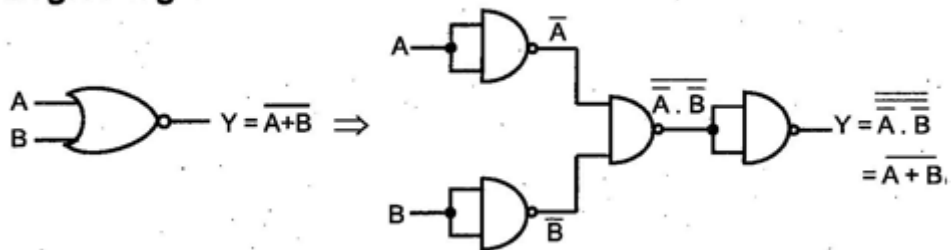
**Logic Equation**

$$Y = \overline{A+B}$$

$$= \overline{A \cdot B} \quad (\because \overline{A+B} = \overline{A \cdot B} \text{ Demorgan's first theorem})$$

$$= \overline{\overline{\overline{A \cdot B}}} \quad (\because \overline{\overline{A}} = A \text{ laws of complementation})$$

**Logic Diagram**

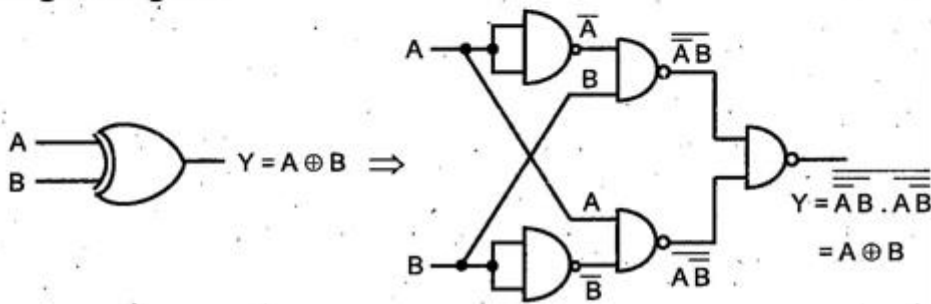


**EX-OR gate using only NAND gates**

**Logic Equation**

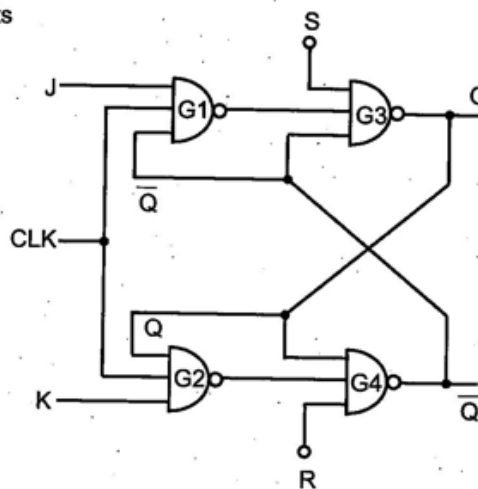
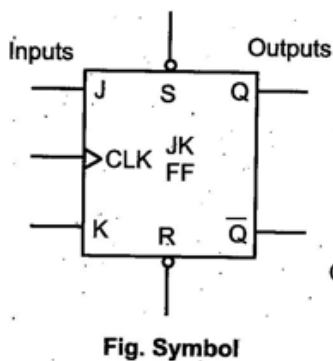
$$\begin{aligned}
 Y &= A \oplus B \\
 &= \bar{A}B + A\bar{B} \\
 &= \overline{\overline{\bar{A}B + A\bar{B}}} \quad (\because \overline{\overline{A}} = A \text{ laws of complementation}) \\
 &= \overline{\bar{A}B \cdot A\bar{B}} \quad (\because \overline{A+B} = \bar{A} \cdot \bar{B} \text{ Demorgan's first theorem})
 \end{aligned}$$

**Logic Diagram**



**15. (a) Explain the JK flip flop with its symbol diagram, circuit diagram, truth tables, excitation table and its operations. (14 Marks)**  
**(Symbol – 2 Marks, Circuit diagram – 2 Marks, Truth Table – 3 Marks, Excitation Table – 3 Marks, Operation – 4 Marks)**

The JK flip flop has three inputs J, K, CLK and two outputs Q, Q. Also, it has Set (S) and Reset (R) asynchronous inputs. They are used to set or reset the flip flop initially. The positive edge triggered JK flip flop is shown in figure.



The bubbles shown in S and R inputs represent the active low inputs. The signal is active when it is 0. When S = 0, the flip flop is SET and when R = 0, the flip flop is RESET.

### Operation

During the positive edge of the clock pulse,

- ✓ When J = 0 and K = 0, the outputs are not changed. This condition is called No change.
- ✓ When J = 0 and K = 1, Q = 0 and  $\bar{Q} = 1$ . This condition is called RESET.
- ✓ When J = 1 and K = 0, Q = 1 and  $\bar{Q} = 0$ . This condition is called SET.
- ✓ When J = 1 and K = 1, the output will toggle repeatedly.





CLK	Inputs		Outputs		Condition
	J	K	Q	$\bar{Q}$	
	0	0	Previous value	Previous value	No change
	0	1	0	1	Reset
	1	0	1	0	Set
	1	1	Complement of previous value	Complement of previous value	Toggle

Table. Truth Table

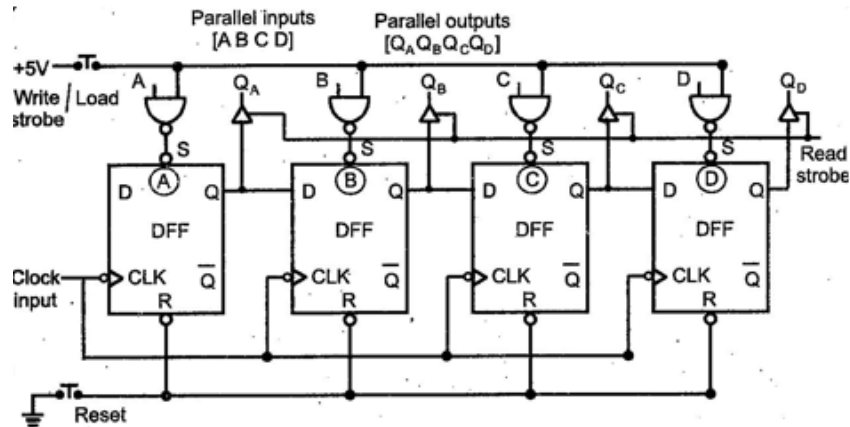
Q Output		Inputs	
Present State	Next State	J <sub>n</sub>	K <sub>n</sub>
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

The condition J = 1 and K = 1 is used to toggle the flip flop. Toggle means that if the previous output is 0, the present output will be 1; similarly, if the previous output is 1, the present output will be 0. Hence the toggle condition in JK flip flop eliminates the NOT USED (forbidden) condition of SR flip flop.

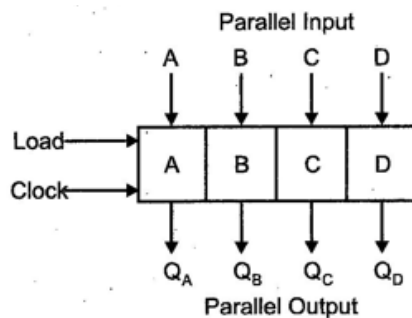
**15. (b) Draw the logic diagram of 4 bit parallel in parallel out shift register. Explain its four modes of operation. (14 Marks)**

**(Diagram – 7 Marks, Operation – 7 Marks)**

In PIPO shift register, the data is entered and retrieved in parallel from (all the bits simultaneously). It is constructed by using four D flip flops.



**Fig. Logic Diagram of 4 - bit PIPO Shift Register**



**Fig. Logic Symbol of 4 - bit PIPO**

**Input data:** The parallel input data A, B, C, D are given to the set terminal of the A, B, C, D flip flops simultaneously through NAND gates. The NAND gates are enabled by Load / Write strobe switch.

**Clock input:** All flip flops are connected in synchronous mode. i.e, clock input is applied to all the flip flops simultaneously.

**Reset:** The Reset (R) inputs of all the flip flops are connected to ground through Master Reset Switch.

The output of each FF is given to the input of next flip flop.

**Output:**

The Q output of all the flip flops are taken as the parallel output data  $Q_A$   $Q_B$   $Q_C$   $Q_D$

## Operation

Consider the input data [ABCD]=0111.

### Write Operation (Input)

It is similar to PISO shift Register.

- ✓ When the Master Reset Switch is pressed, all the flip flops are cleared.
- ✓ 4-bits of data is given to the parallel terminals A, B, C, D when the load / write strobe switch is pressed. The 4-bits of data is stored in the four flip flops.  
i.e.,  $Q_A Q_B Q_C Q_D = 0111$
- ✓ Disable Load/Write strobe.

### Read Operation (Output)

It is similar to SIPO shift register.

When the Read strobe is enabled, the 4 bits of data can be retrieved from the shift register without applying any clock pulse. The data is taken from the Q outputs of all the flip flops ( $Q_A Q_B Q_C Q_D$ ) simultaneously through the tristate buffer.

$$Q_A Q_B Q_C Q_D = 0111$$

### Timing Diagram

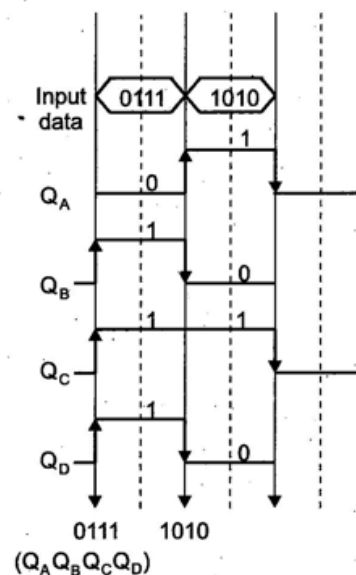


Fig. Timing diagram of PIPO shift register

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